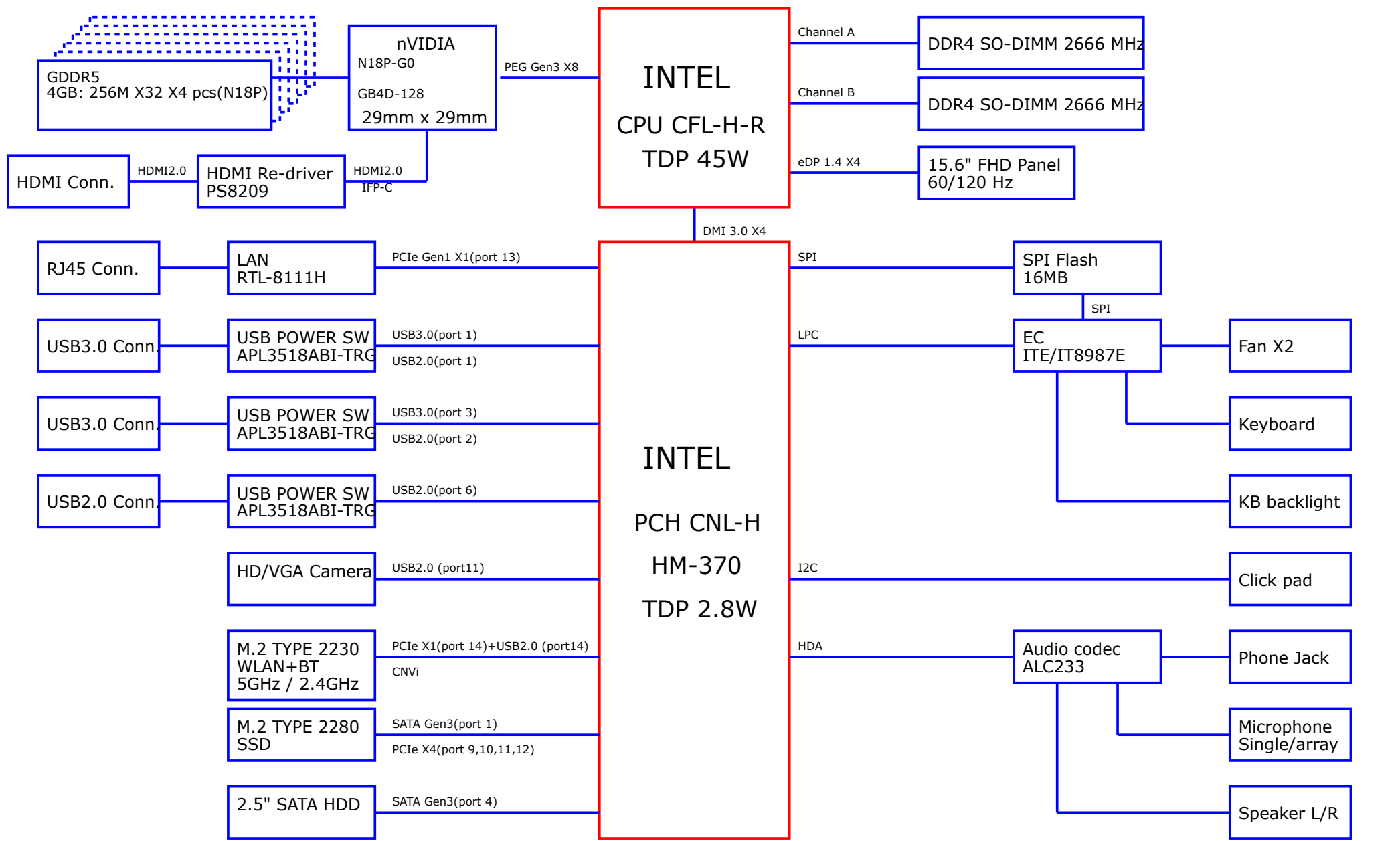


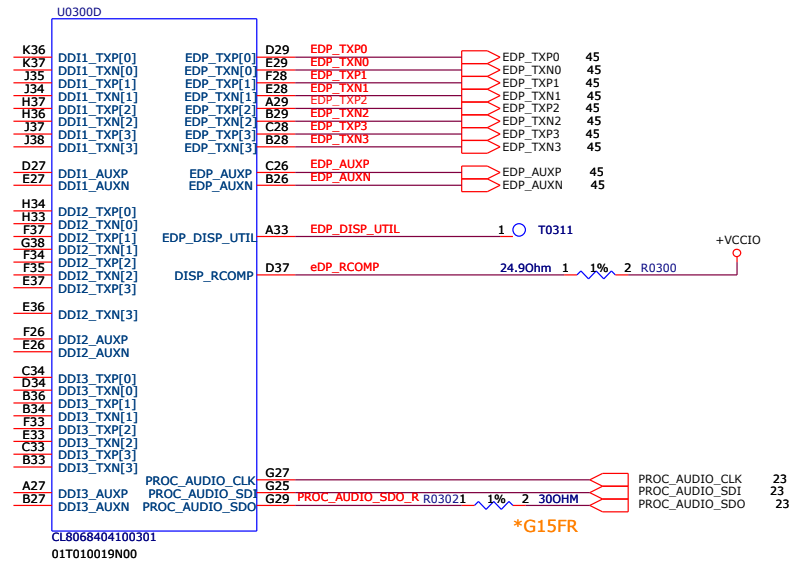
FX505GT Block Diagram





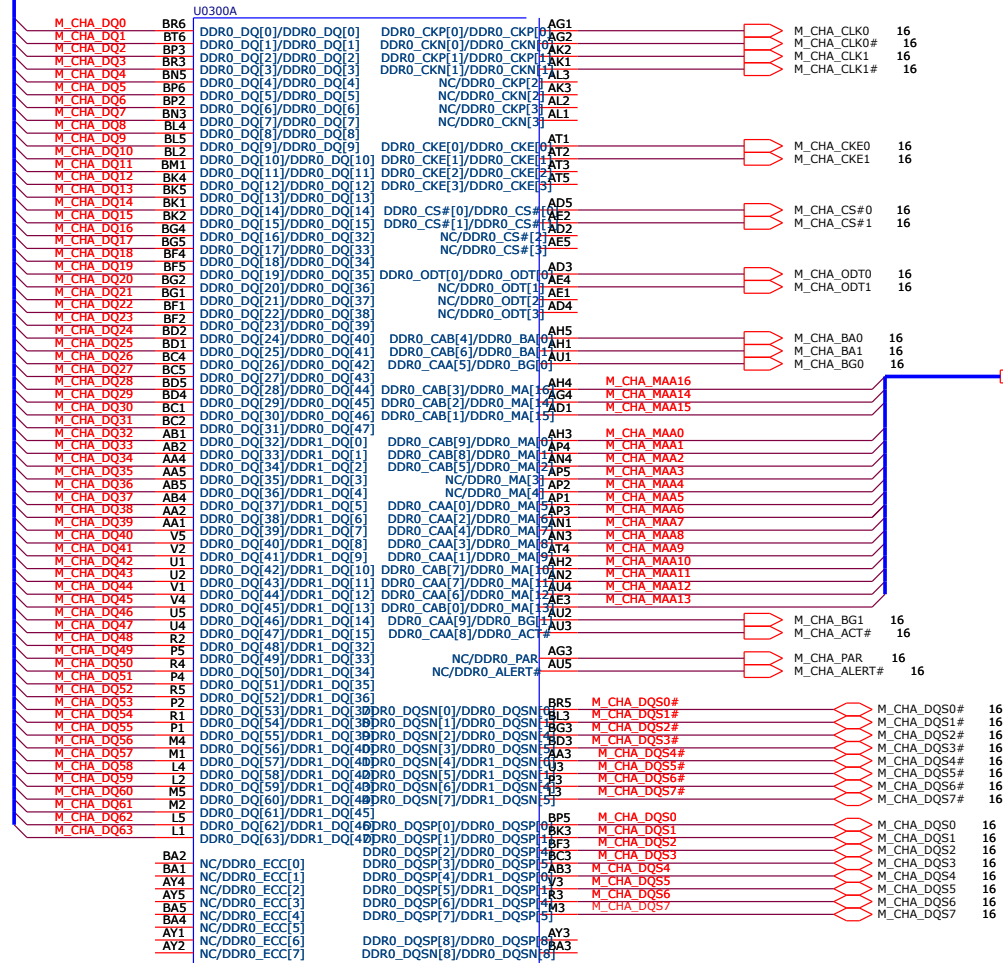
I2C_Port	Module	DEVICE	7-bit addr
I2C_0	TOUCH PAD		
I2C_1			
SMBUS	DDR Channel A(CON1601)		
	DDR Channel B(CON1701)		
SMBUS0 (EC)	BATTERY		0X0B
	CHARGE IC	BQ24780SRUYR	0X09
SMBUS1 (EC)			
	GPU		







16 M\_CHA\_DQ[0..63]



CL8068404100301  
01T010019N00



17 M\_CHB\_DQ[0..63]

+1P2V +1P2V 7,10,16,17,18,24,57,83

U03008

M\_CHB\_DQ0 BT11  
M\_CHB\_DQ1 BR11  
M\_CHB\_DQ2 BT9  
M\_CHB\_DQ3 BR8  
M\_CHB\_DQ4 BP11  
M\_CHB\_DQ5 BN11  
M\_CHB\_DQ6 BP8  
M\_CHB\_DQ7 BN8  
M\_CHB\_DQ8 BL12  
M\_CHB\_DQ9 BL11  
M\_CHB\_DQ10 BL8  
M\_CHB\_DQ11 B38  
M\_CHB\_DQ12 B311  
M\_CHB\_DQ13 B310  
M\_CHB\_DQ14 BL7  
M\_CHB\_DQ15 B37  
M\_CHB\_DQ16 BG11  
M\_CHB\_DQ17 BG10  
M\_CHB\_DQ18 BG8  
M\_CHB\_DQ19 BF8  
M\_CHB\_DQ20 BF11  
M\_CHB\_DQ21 BF10  
M\_CHB\_DQ22 BG7  
M\_CHB\_DQ23 BF7  
M\_CHB\_DQ24 BB11  
M\_CHB\_DQ25 BC11  
M\_CHB\_DQ26 BB8  
M\_CHB\_DQ27 BC8  
M\_CHB\_DQ28 BC10  
M\_CHB\_DQ29 BB10  
M\_CHB\_DQ30 BC7  
M\_CHB\_DQ31 BB7  
M\_CHB\_DQ32 AA11  
M\_CHB\_DQ33 AA10  
M\_CHB\_DQ34 AC11  
M\_CHB\_DQ35 AC10  
M\_CHB\_DQ36 AA7  
M\_CHB\_DQ37 AA8  
M\_CHB\_DQ38 AC8  
M\_CHB\_DQ39 AC7  
M\_CHB\_DQ40 W8  
M\_CHB\_DQ41 W7  
M\_CHB\_DQ42 V10  
M\_CHB\_DQ43 V11  
M\_CHB\_DQ44 W11  
M\_CHB\_DQ45 W10  
M\_CHB\_DQ46 V7  
M\_CHB\_DQ47 V8  
M\_CHB\_DQ48 R11  
M\_CHB\_DQ49 P11  
M\_CHB\_DQ50 P7  
M\_CHB\_DQ51 R8  
M\_CHB\_DQ52 R10  
M\_CHB\_DQ53 P10  
M\_CHB\_DQ54 R7  
M\_CHB\_DQ55 P8  
M\_CHB\_DQ56 L11  
M\_CHB\_DQ57 M11  
M\_CHB\_DQ58 L7  
M\_CHB\_DQ59 M8  
M\_CHB\_DQ60 L10  
M\_CHB\_DQ61 M10  
M\_CHB\_DQ62 M7  
M\_CHB\_DQ63 L8

AW11 NC/DDR1\_ECC[0]  
AY11 NC/DDR1\_ECC[1]  
AW8 NC/DDR1\_ECC[2]  
AY10 NC/DDR1\_ECC[3]  
AW10 NC/DDR1\_ECC[4]  
AY7 NC/DDR1\_ECC[5]  
AW7 NC/DDR1\_ECC[6]  
NC/DDR1\_ECC[7]

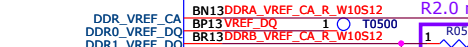
DDR1\_CKP[0]/DDR1\_CKP[9] AM9  
DDR1\_CKN[0]/DDR1\_CKN[9] AN9  
DDR1\_CKP[1]/DDR1\_CKP[10] AM8  
DDR1\_CKN[1]/DDR1\_CKN[10] AM10  
NC/DDR1\_CKP[2] AJ10  
NC/DDR1\_CKP[3] AJ11  
NC/DDR1\_CKN[3] AJ11  
DDR1\_CKE[0]/DDR1\_CKE[9] AT8  
DDR1\_CKE[1]/DDR1\_CKE[10] AT10  
DDR1\_CKE[2]/DDR1\_CKE[11] AT11  
DDR1\_CKE[3]/DDR1\_CKE[12] AT11  
DDR1\_CS#[0]/DDR1\_CS#[9] AF11  
DDR1\_CS#[1]/DDR1\_CS#[10] AF7  
NC/DDR1\_CS#[2] AE10  
NC/DDR1\_CS#[3] AE10  
DDR1\_ODT[0]/DDR1\_ODT[9] AF7  
NC/DDR1\_ODT[1] AE8  
NC/DDR1\_ODT[2] AE11  
NC/DDR1\_ODT[3] AE11  
DDR1\_CAB[3]/DDR1\_CAB[10] AH10  
DDR1\_CAB[6]/DDR1\_CAB[13] AH11  
DDR1\_CAB[1]/DDR1\_CAB[14] AF8  
DDR1\_CAB[4]/DDR1\_CAB[11] AH8  
DDR1\_CAB[5]/DDR1\_CAB[12] AH9  
DDR1\_CAB[8]/DDR1\_CAB[15] AK6  
DDR1\_CAB[9]/DDR1\_CAB[16] AK5  
DDR1\_CAB[12]/DDR1\_CAB[19] AL5  
NC/DDR1\_CAB[13] AL6  
DDR1\_CAA[0]/DDR1\_CAA[7] AN7  
DDR1\_CAA[1]/DDR1\_CAA[8] AN10  
DDR1\_CAA[3]/DDR1\_CAA[10] AN8  
DDR1\_CAA[4]/DDR1\_CAA[11] AN11  
DDR1\_CAB[7]/DDR1\_CAB[14] AN11  
DDR1\_CAA[6]/DDR1\_CAA[13] AR10  
DDR1\_CAB[10]/DDR1\_CAB[17] AF9  
DDR1\_CAA[9]/DDR1\_CAA[16] AT9  
DDR1\_CAA[8]/DDR1\_CAA[15] AR7  
NC/DDR1\_PAR# AJ7  
NC/DDR1\_ALERT# AR8

571391\_PDG\_P.134  
All VREF traces should be at least 20 mils wide with 20 mils spacing to other signals/planes

571483\_RVP\_TDK\_SCH\_P.27



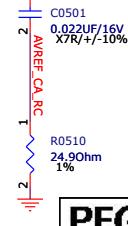
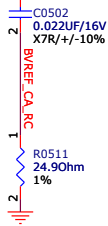
571483\_CFL\_H\_DDR4\_RVP\_TDK\_SCH\_Rev0p9\_P.16/224



Channel B



Channel A





+VCCIO

+VCCIO

3,7,10,94

70 PCIEB\_RXN[15:0]  
70 PCIEB\_RXP[15:0]

PEG Lane reversal

PCIEG\_TXN[15:0] 70  
PCIEG\_TXP[15:0] 70

571483\_CFL\_H\_DDR4\_RVP\_TDK\_SCH\_Rev0p9\_P.18/224

+VCCIO R0600 1 1% 2 24.90hm PEG\_RCOMP G2 PEG\_RCOMP

NOTE:  
W/S=12/15 mil, length<400mil

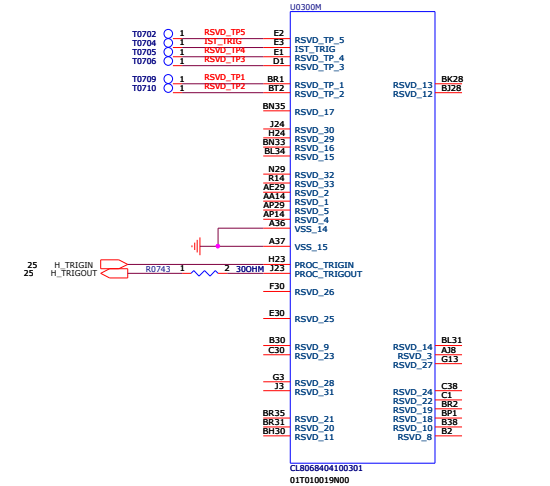
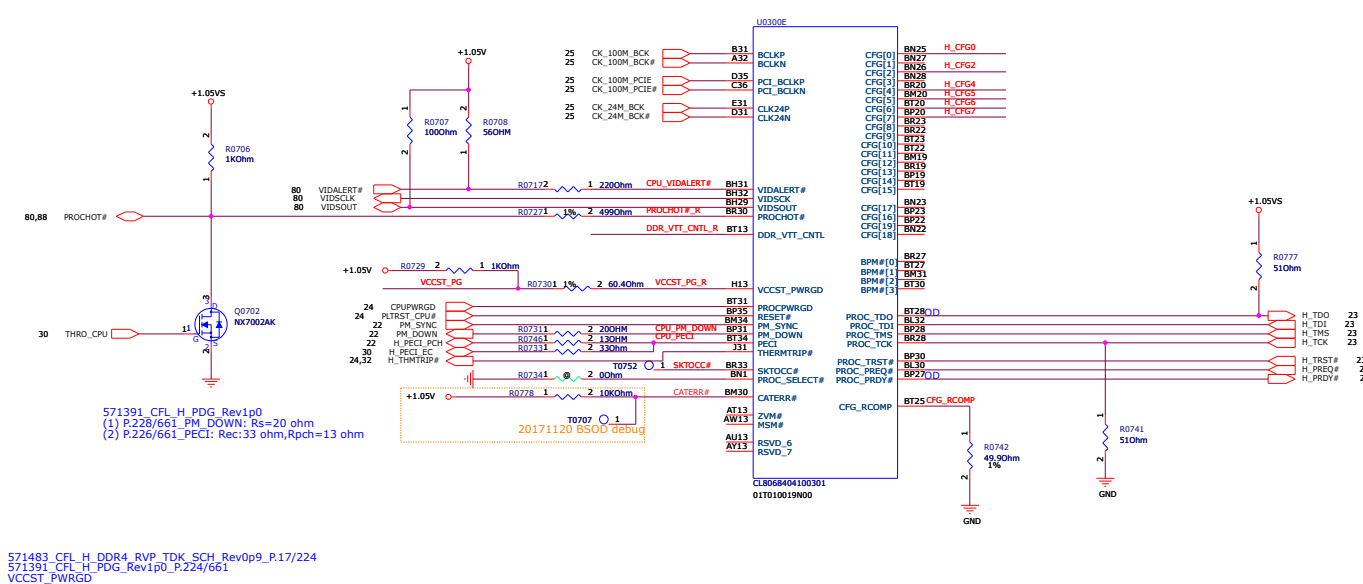
20	DMI_RXP0	D8	DMI_RXP[0]	DMI_TXP[0]	B8	DMI_TXP0	20
20	DMI_RXN0	E8	DMI_RXN[0]	DMI_TXN[0]	A8	DMI_TXN0	20
20	DMI_RXP1	E6	DMI_RXP[1]	DMI_TXP[1]	C6	DMI_TXP1	20
20	DMI_RXN1	F6	DMI_RXN[1]	DMI_TXN[1]	B6	DMI_TXN1	20
20	DMI_RXP2	D5	DMI_RXP[2]	DMI_TXP[2]	B5	DMI_TXP2	20
20	DMI_RXN2	E5	DMI_RXN[2]	DMI_TXN[2]	A5	DMI_TXN2	20
20	DMI_RXP3	J8	DMI_RXP[3]	DMI_TXP[3]	D4	DMI_TXP3	20
20	DMI_RXN3	J9	DMI_RXN[3]	DMI_TXN[3]	B4	DMI_TXN3	20

CL8068404100301  
01T010019N00



+VCCIO	3,6,10,94
+1.05V	10,24,32,57,80,91
+1.05V	10,57,91
+3VSUS	21,22,23,24,26,28,30,31,33,36,48,51,53,68,74,81,88,92,96
+3VS	16,21,22,23,24,28,30,31,32,33,36,44,45,48,50,51,57,74,87,88,91,92,96
+1P2V	10,16,17,18,24,57,83

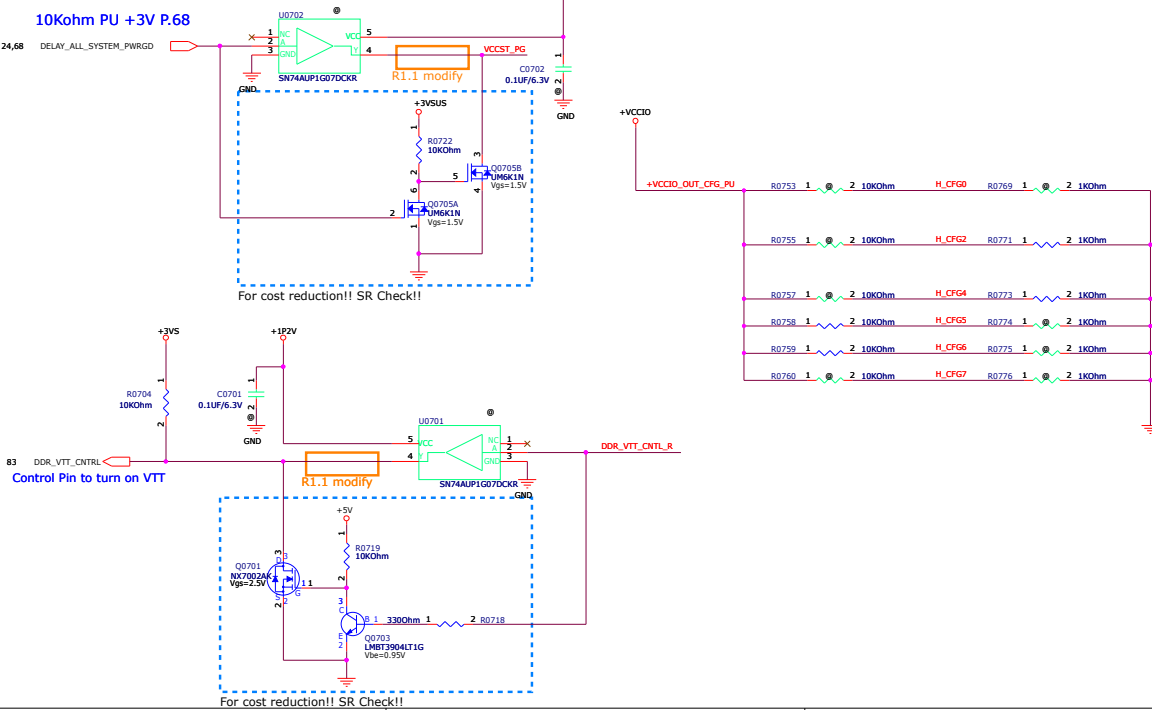
570805\_CFL\_Protessor\_EDS\_Vol1\_Rev\_1.4\_P.123/156  
 The following are the general types of reserved (RSVD) signals and connection guidelines:  
 RSVD : these signals should not be connected  
 RSVD\_TP: these signals should be routed to a test point  
 RSVD\_NCTF :these signals are non-critical to function and may be left unconnected



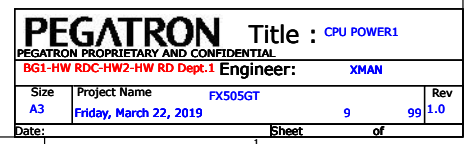
570805\_CFL\_Protessor\_EDS\_Vol1\_Rev\_1.4\_p.117/156

Table 6-7. Reset and Miscellaneous Signals (Sheet 1 of 2)

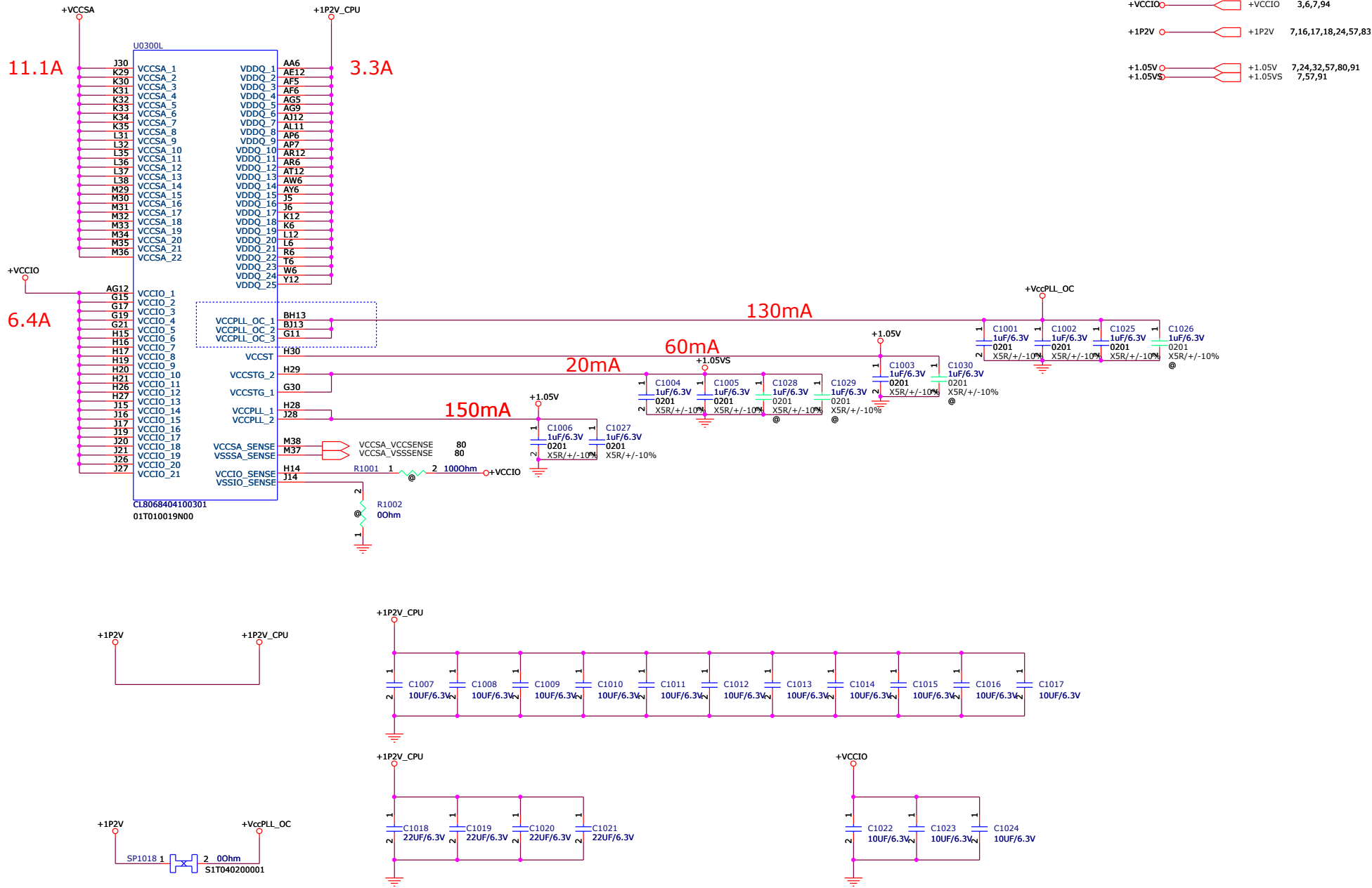
Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
CFG[19:0]	<p><b>Configuration Signals:</b> The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired.</p> <p>Intel recommends placing test points on the board for CFG pins.</p> <ul style="list-style-type: none"> <li><b>CFG[0]:</b> Stall reset sequence after PCU PLL lock until de-asserted:               <ul style="list-style-type: none"> <li>1 = (Default) Normal Operation; No stall.</li> <li>0 = Stall.</li> </ul> </li> <li><b>CFG[1]:</b> Reserved configuration lane.</li> <li><b>CFG[2]:</b> PCI Express* Static x16 Lane Numbering Reversal.               <ul style="list-style-type: none"> <li>1 = Normal operation</li> <li>0 = Lane numbers reversed.</li> </ul> </li> <li><b>CFG[3]:</b> Reserved configuration lane.</li> <li><b>CFG[4]:</b> eDP enable:               <ul style="list-style-type: none"> <li>1 = Disabled.</li> <li>0 = Enabled.</li> </ul> </li> <li><b>CFG[6:5]:</b> PCI Express* Bifurcation               <ul style="list-style-type: none"> <li>00 = 1 x8, 2 x4 PCI Express*</li> <li>01 = reserved</li> <li>10 = 2 x8 PCI Express*</li> <li>11 = 1 x16 PCI Express*</li> </ul> </li> <li><b>CFG[7]:</b> PEG Training:               <ul style="list-style-type: none"> <li>1 = (default) PEG Train Immediately following RESET# de assertion.</li> <li>0 = PEG Wait for BIOS for training.</li> </ul> </li> <li><b>CFG[19:8]:</b> Reserved configuration lanes.</li> </ul>	I	GTL	SE	All Processor Lines. CFG[2], CFG[6:5] and CFG[7] are relevant for H and S-Processor Line only and test point may be placed on the board for them.











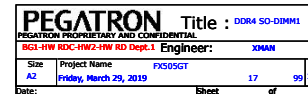


## 20180212 SWAP





+1P2V	○		+1P2V	7,10,16,18,24,57,83
+1P2V_DUAL	○		+1P2V_DUAL	7,10,16,18,24,57,83
+VTT_DDR	○		+VTT_DDR	16,18,57,83
+2P5VPP	○		+2P5VPP	16,18,57,95
+3VS	○		+3VS	7,16,21,22,23,24,28,30,31,32,33,36,44,45,48,50,51,57,74,87,88,89,91,92,96



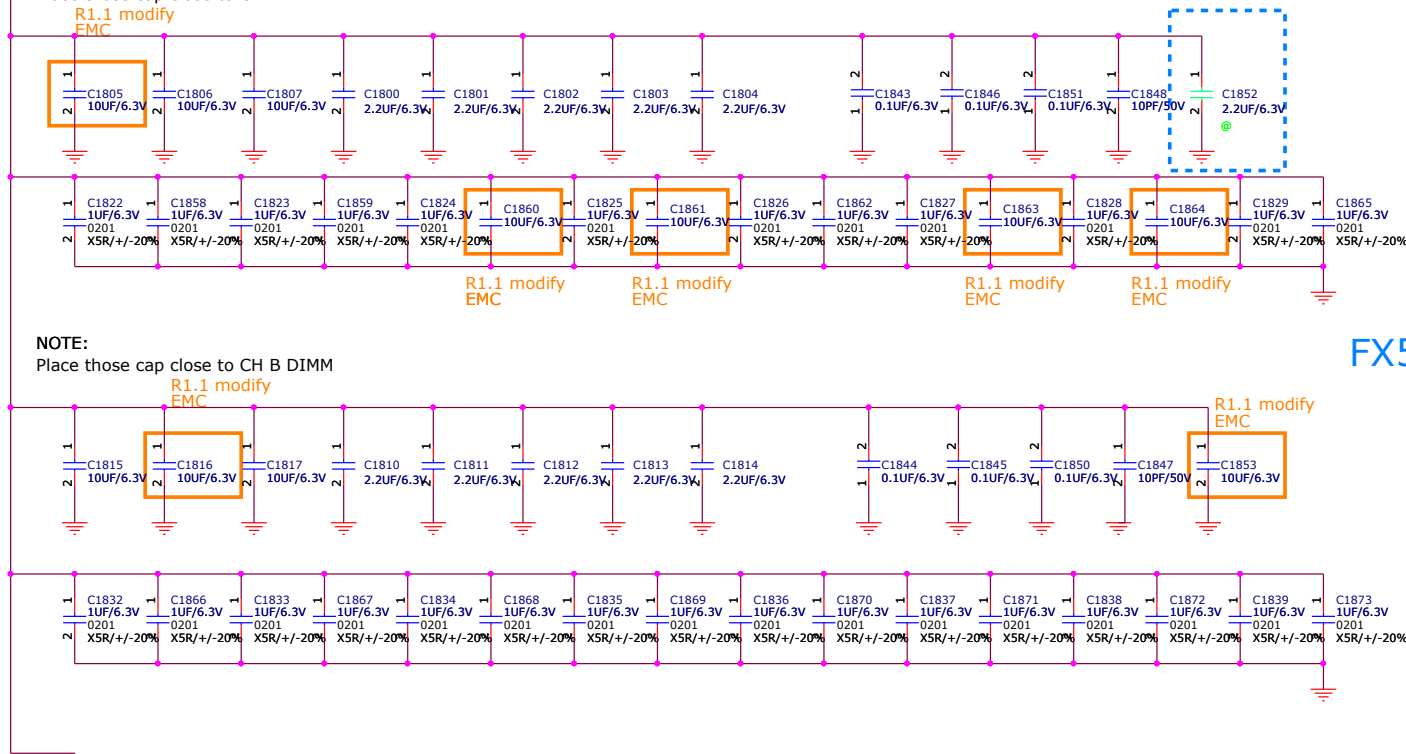


+1P2V\_DUAL

NOTE:  
Place those cap close to CH A DIMM

FX505 RF reserve @20180131

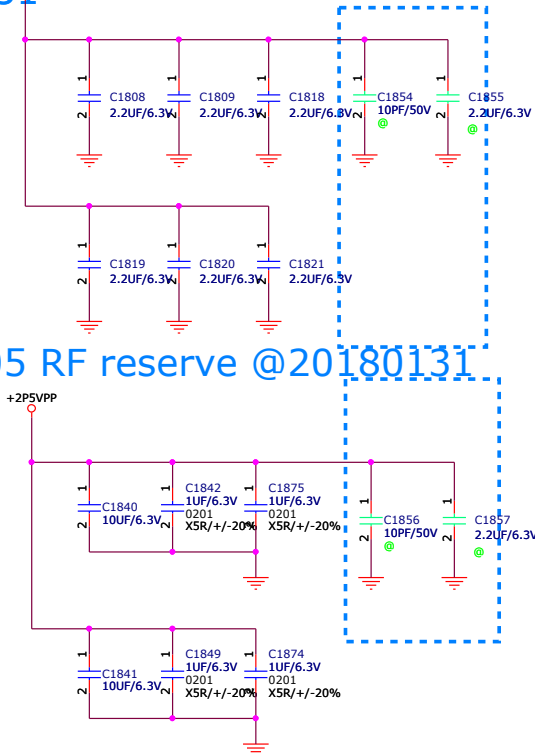
+VTT\_DDR



NOTE:  
Place those cap close to CH B DIMM

FX505 RF reserve @20180131

+2P5VPP



## CFL-H DDR4 SODIMM Decoupling

### DDR4 SODIMM Power Plane Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x $\mu$ F (size)	Note
DDR4 2 Channels SODIMM 1DPC	VDDQ	4 near each side of the DIMM connector close to VDD pins	16x 10 $\mu$ F (0603)	
		4 near each side of the DIMM connector close to VDD pins	16x 1 $\mu$ F (0402)	
		1 placeholder	1x 330 $\mu$ F (7343)	
	VTT	Placed on VTT plane close to DIMM, 1 cap stuffed, 1 placeholder	2x 10 $\mu$ F (0603)	
		Placed on VTT plane close to DIMM	4x 1 $\mu$ F (0402)	
	VPP	DIMM Pin side, 1 per DIMM	2x 10 $\mu$ F (0603)	
		DIMM Pin side, 1 per DIMM	2x 1 $\mu$ F (0402)	
	VDDSPD	Place close to DIMM	2x 0.1 $\mu$ F (0402)	
		Place close to DIMM	2x 2.2 $\mu$ F (0402)	

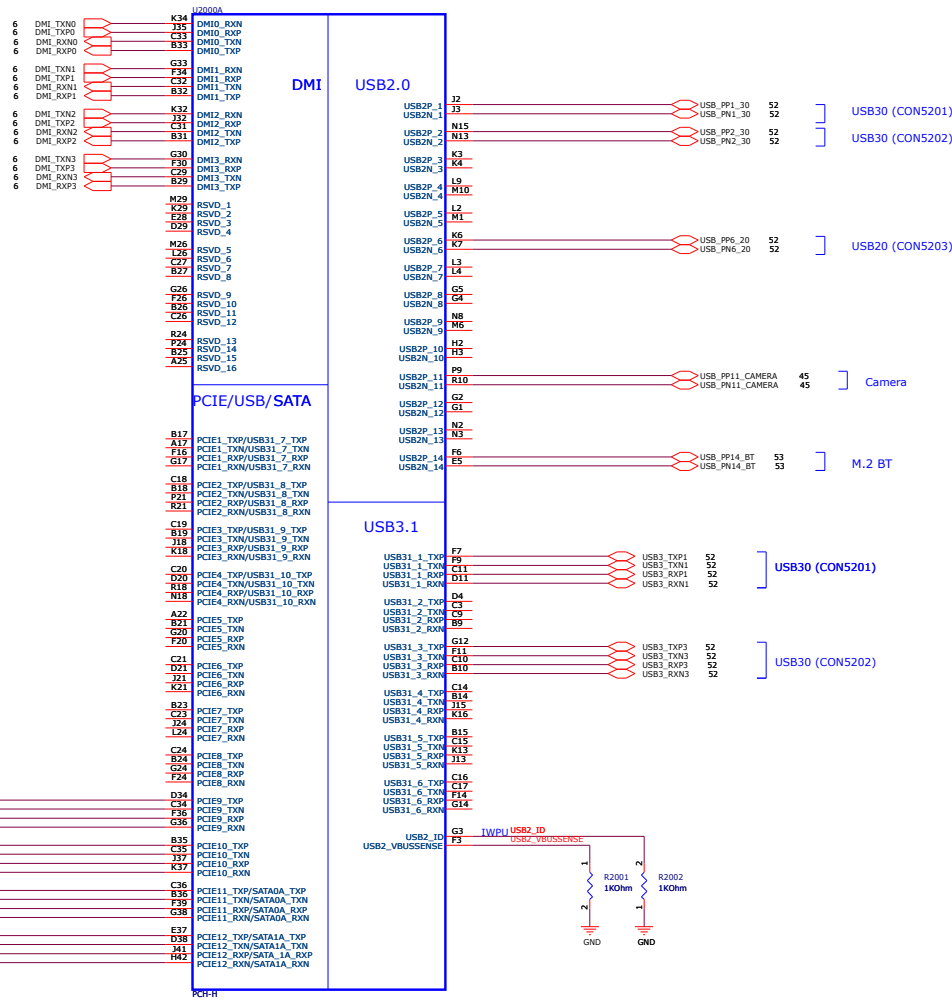
**PEGATRON** Title : DDR4 Caps.  
PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1-HW RDC-HW2-HW RD Dept.1 Engineer: XMAN

Size A3 Project Name FX505GT 18 99 Rev 1.0

Date: Friday, March 29, 2019 Sheet of



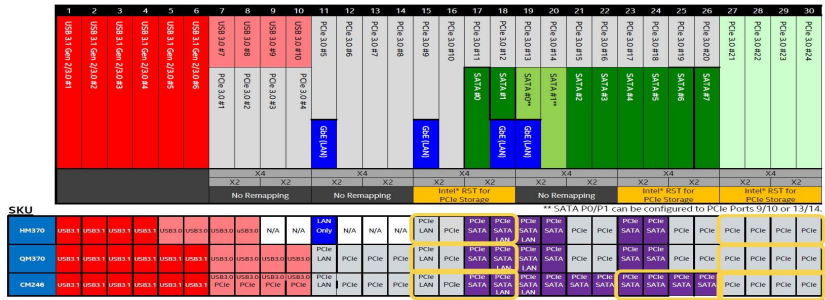


USB30 (CON5201)  
USB30 (CON5202)  
USB20 (CON5203)  
Camera  
M.2 BT

USB3.1 support GEN2  
HM370: 4 ports  
QM370: 6 ports

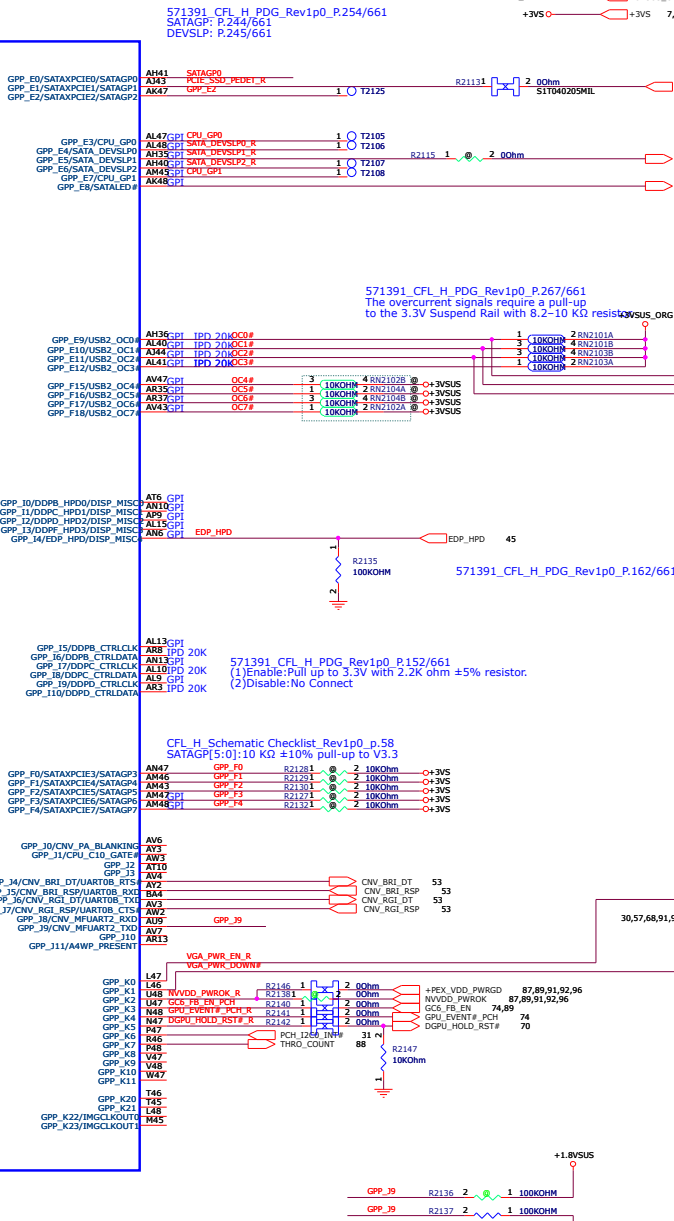
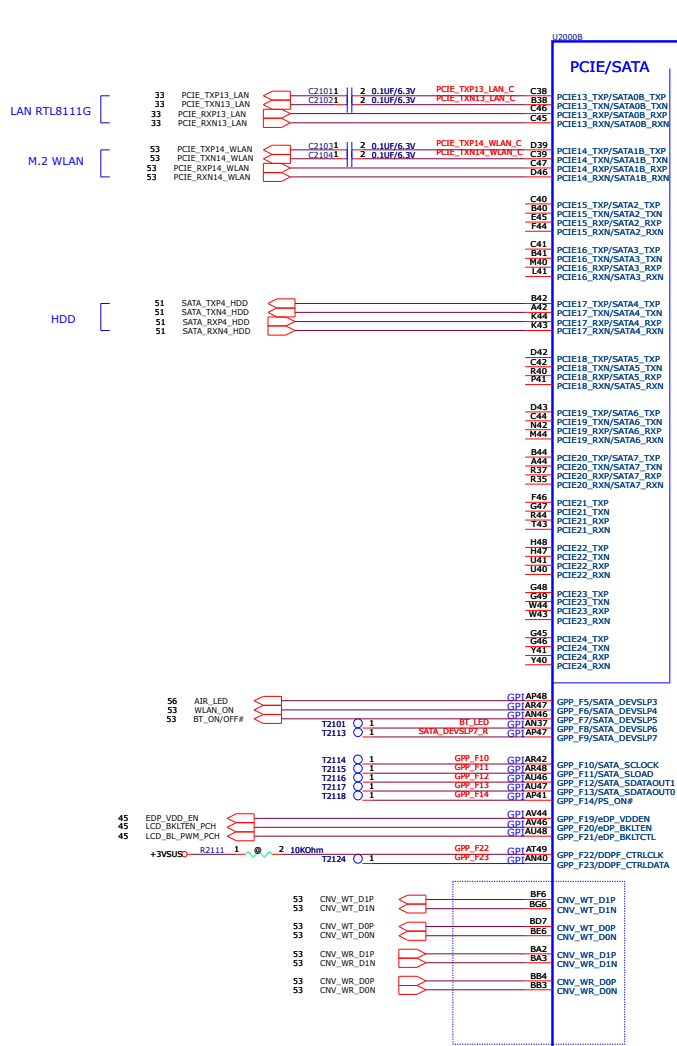
Mobile PCH SKUs	SKU		
	HM370	QM370	CM246
DMI	DMI x4 Gen3	DMI x4 Gen3	DMI x4 Gen3
SATA 3.0 (6 Gbps) Ports	4	4	8
PCIe*	Up to 16 Gen3 lanes	Up to 20 Gen3 lanes	Up to 24 Gen3 lanes
Total USB Ports (Maximum USB 3.1)	14 (8)	14 (10)	14 (10)
Maximum USB 3.1 Ports: Gen 2 (10 Gbps) / Gen 1 (5 Gbps)	4 / 8	6 / 10	6 / 10
Total USB 2.0 Ports	14	14	14
Intel® Smart Sound Technology	YES	YES	YES
Intel® ME 12 Firmware	Consumer	Consumer / Corporate	Consumer / Corporate
Intel® AMT	NO	YES	YES
Intel® Optane™ Memory Support	YES	YES	YES
Intel® Rapid Storage Technology 15	YES	YES	YES
Intel® RST RAID Support	YES	YES	YES
Integrated Intel® Wireless-AC Support	YES	YES	YES
eSPI Chip Select	1	1	1
Intel® Trusted Execution Technology	NO	YES	YES

### Preliminary HSI0 Lane Assignments – CNL PCH-H



- Added 4 new PCIe 3.0 lanes versus KBL-H platform.
- GbE LAN removed from lane 10 and SATA P0/P1 option moved from lanes 15/16 to 19/20 to better balance PHY clocking.

















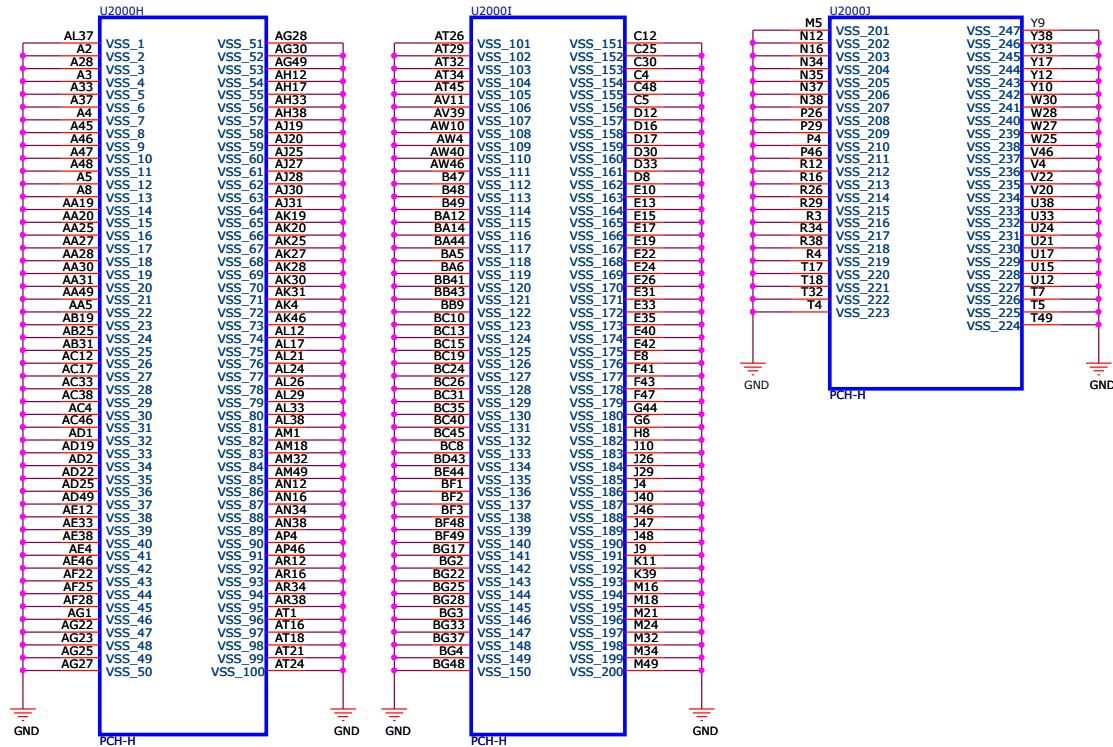






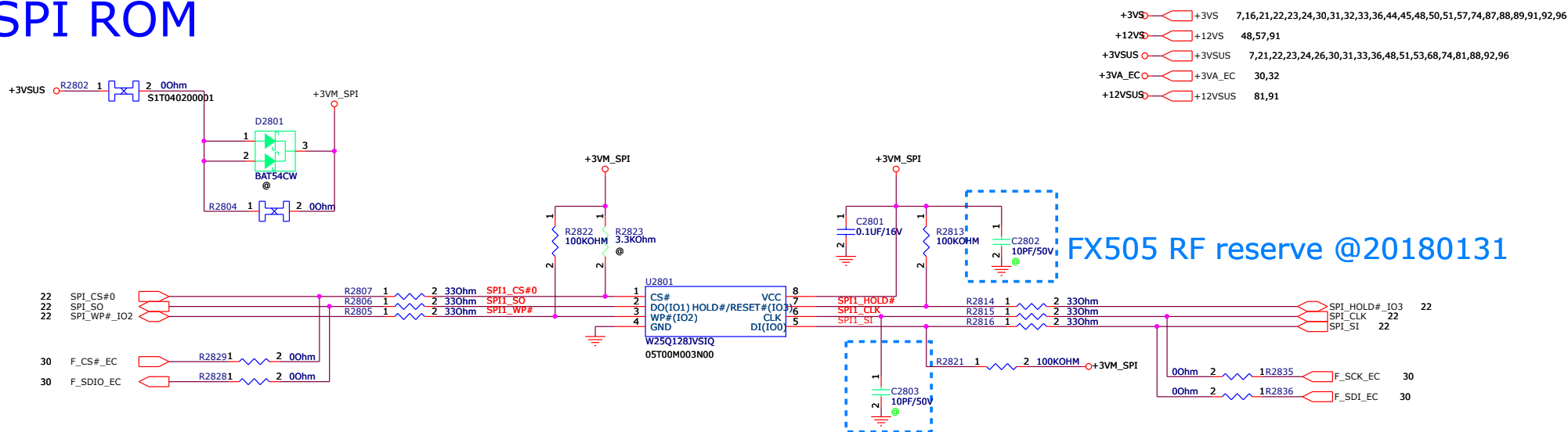




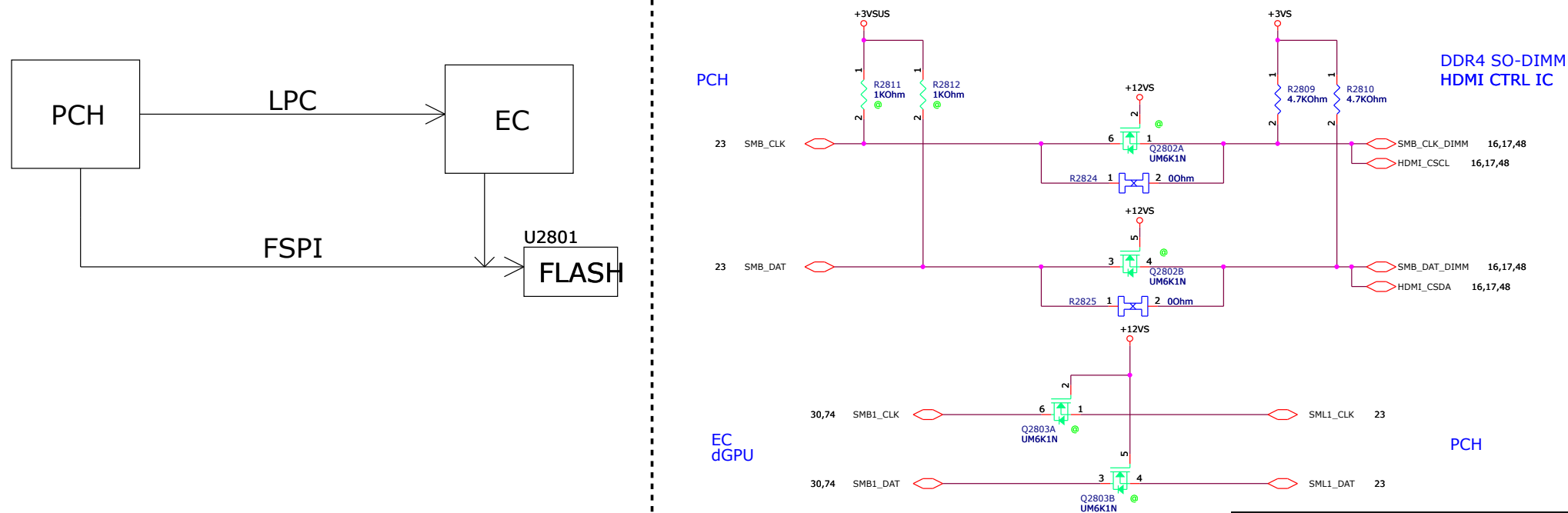




# SPI ROM



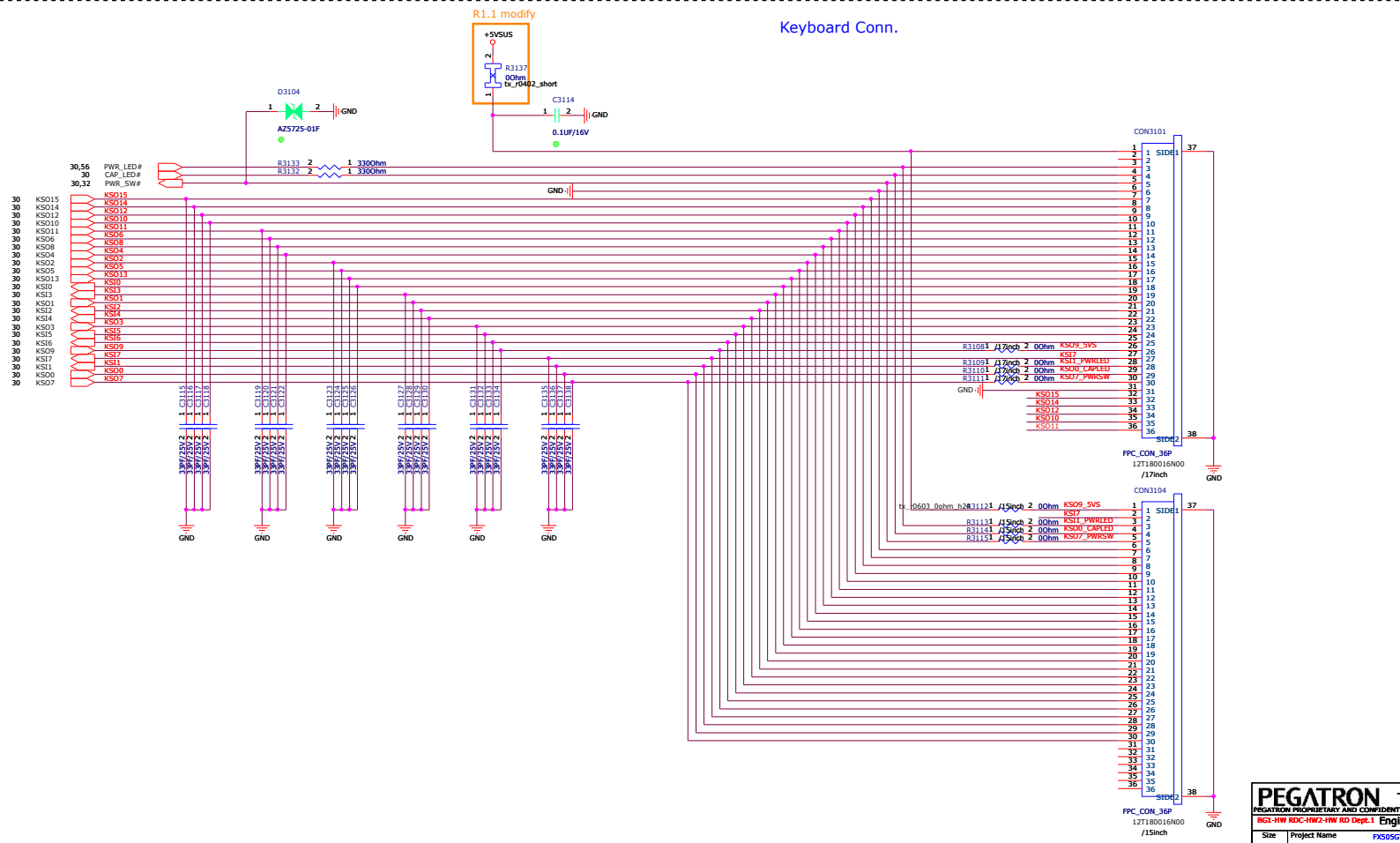
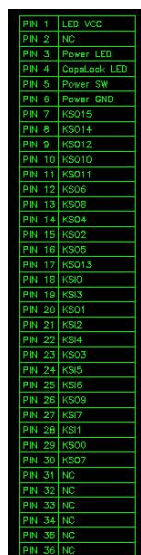
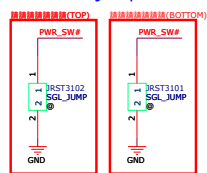
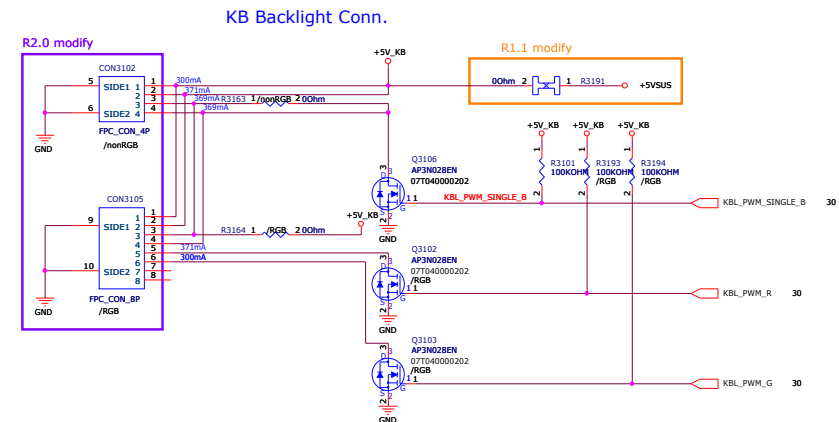
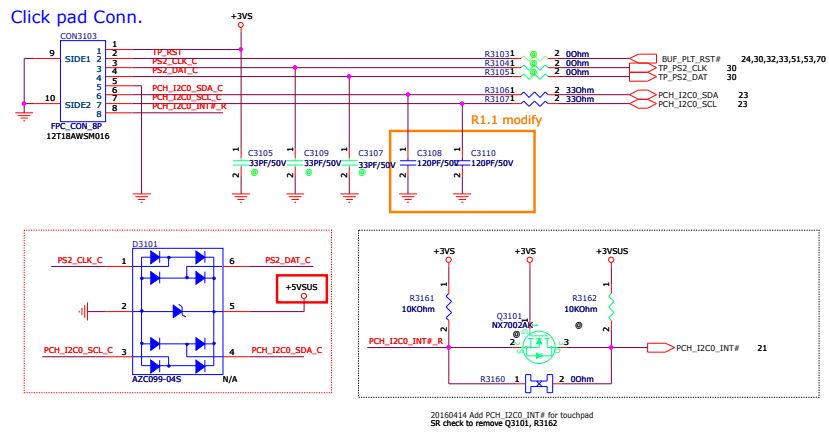
# SMBus





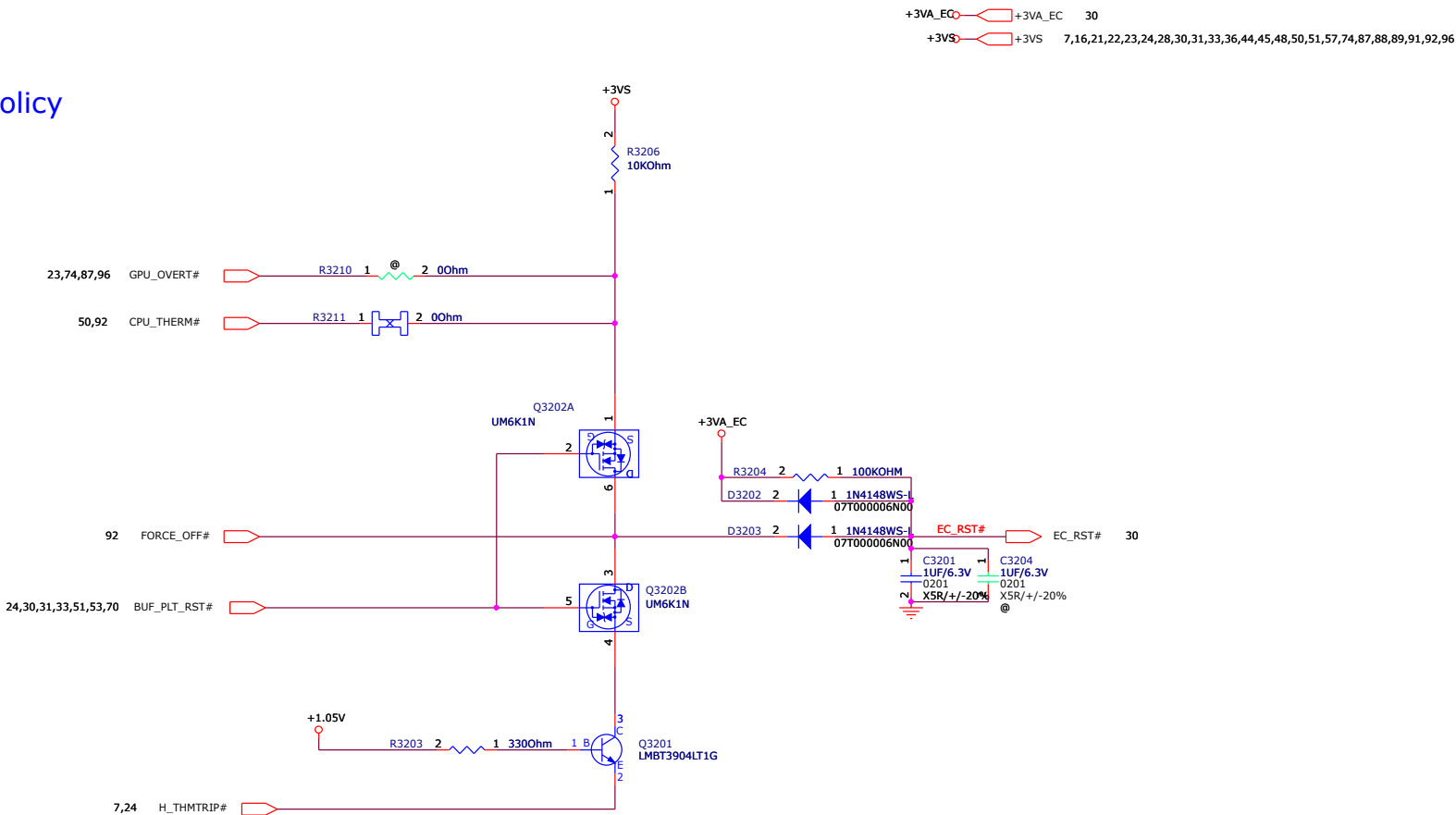




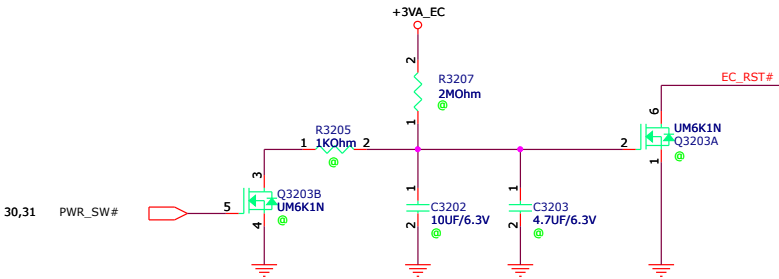




Thermal Policy

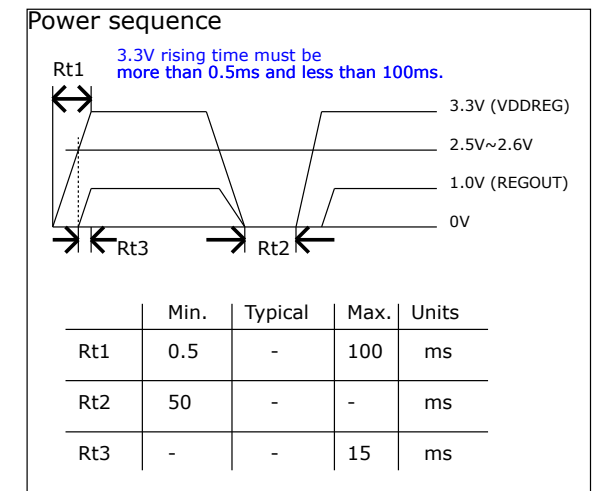
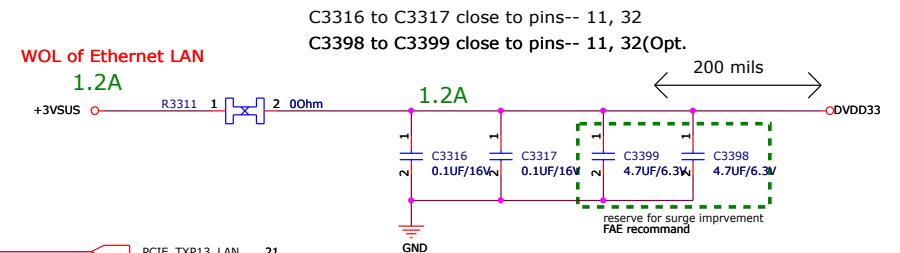
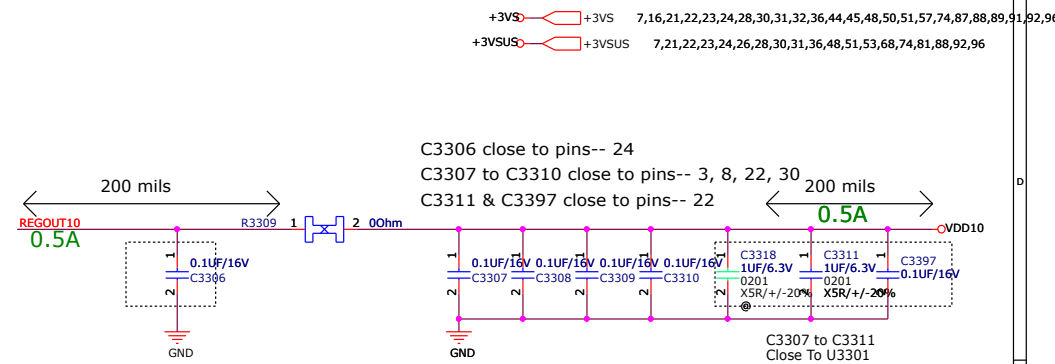
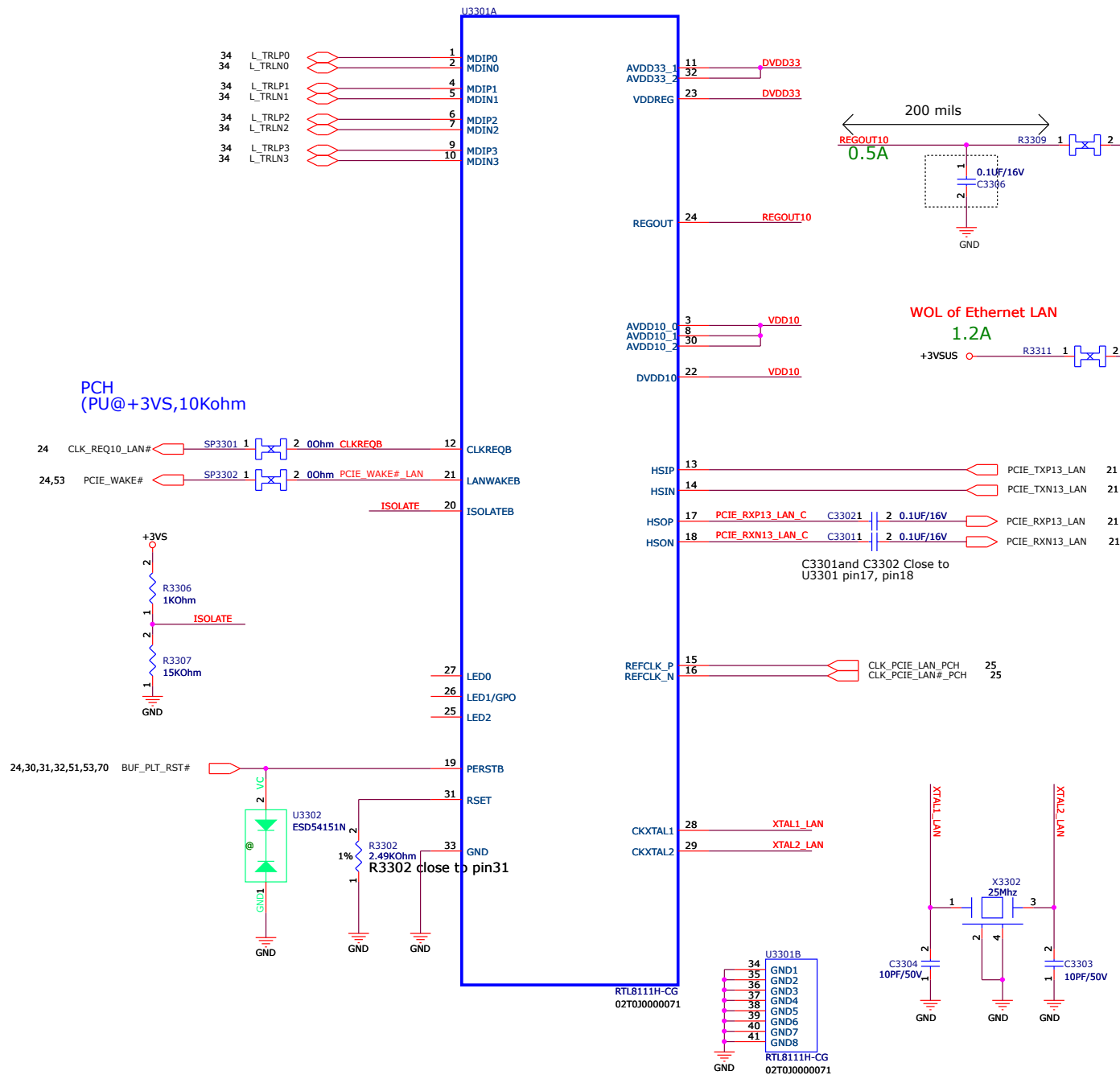


EC reset



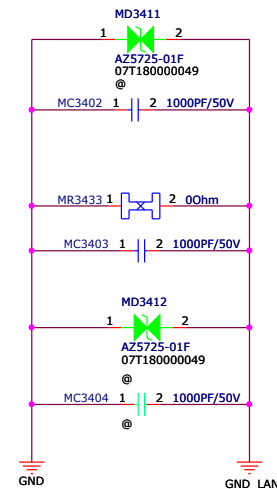
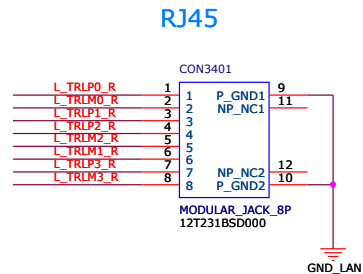
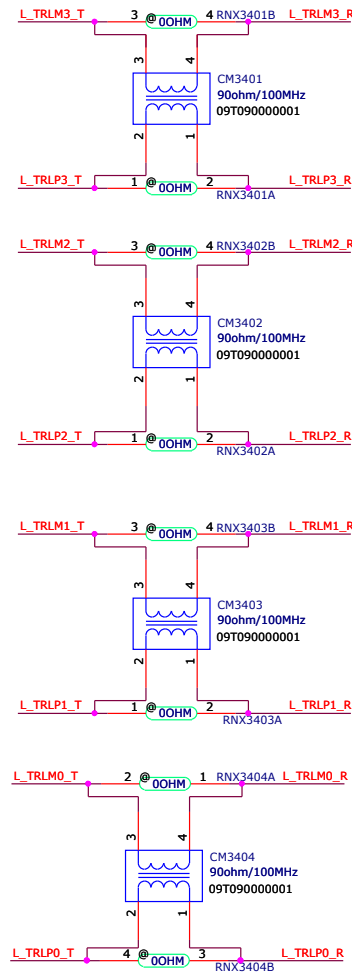
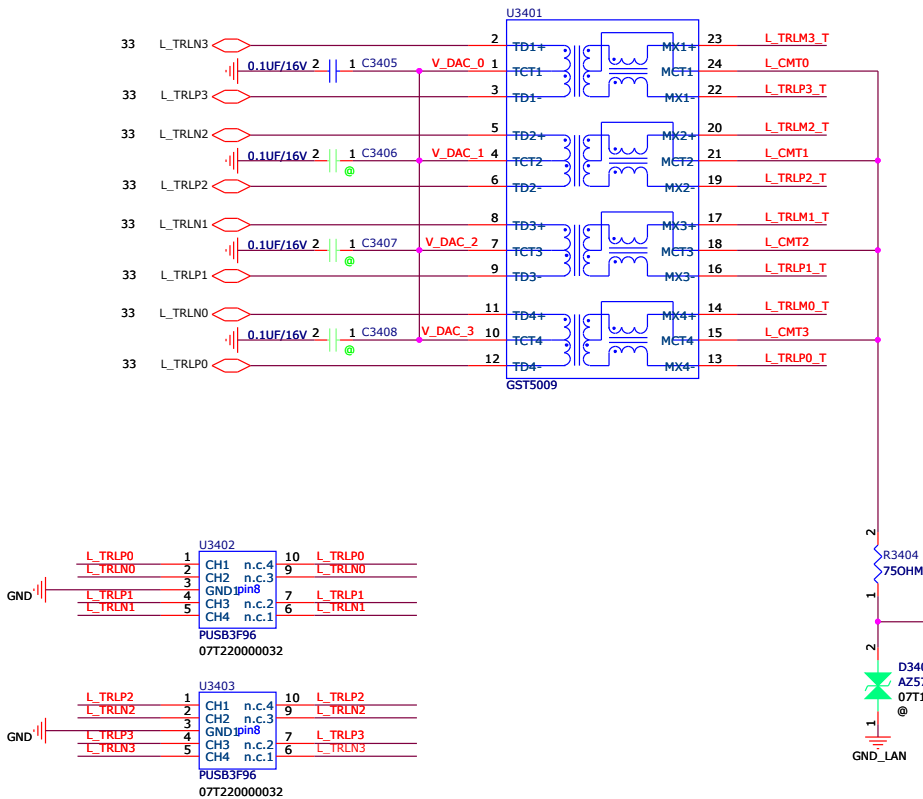
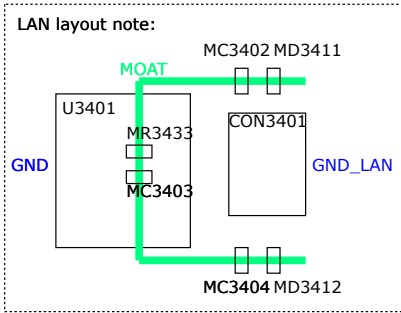


### 33.Realtek RTL8111H



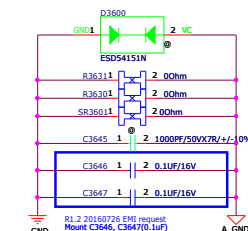
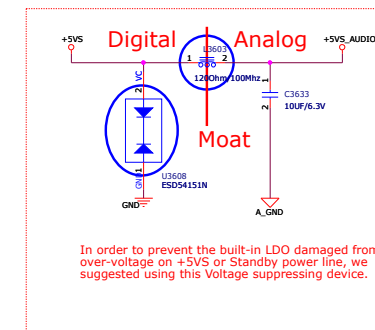
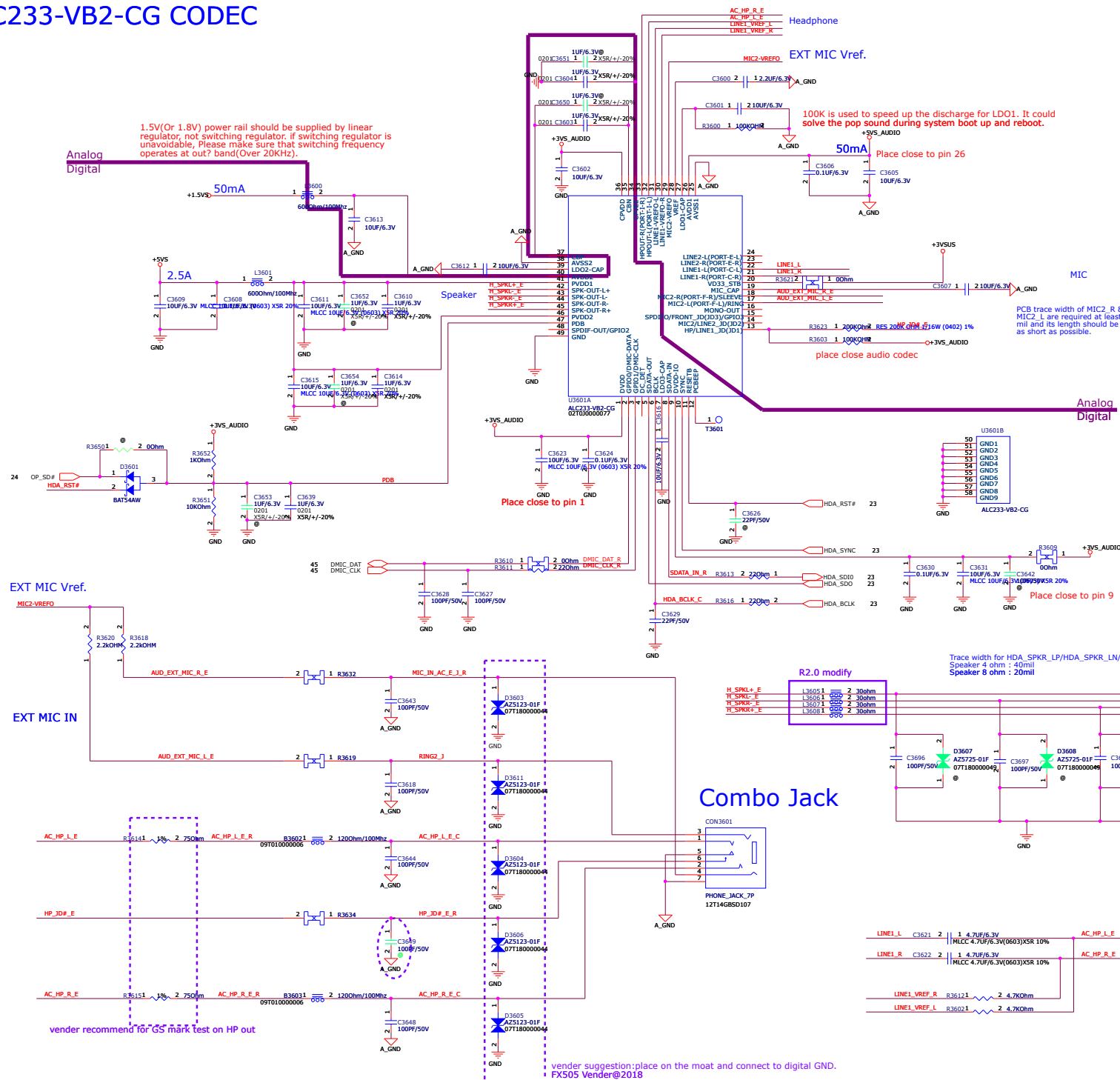


34. Transformer/RJ45

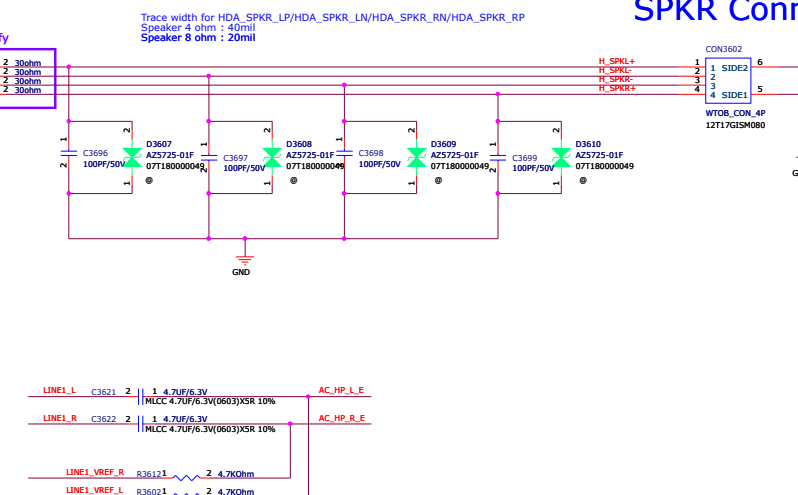




# ALC233-VB2-CG CODEC

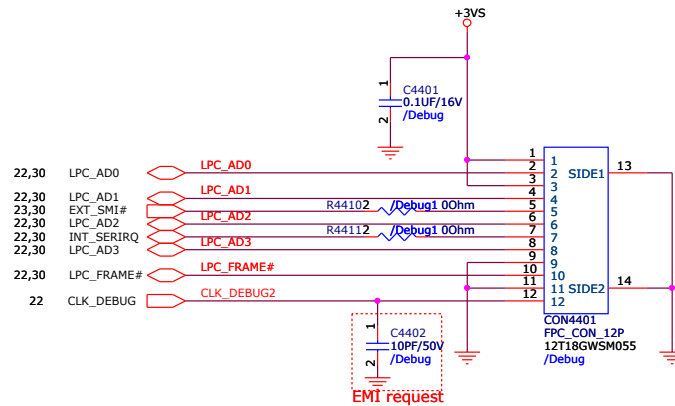


## SPKR Conn.



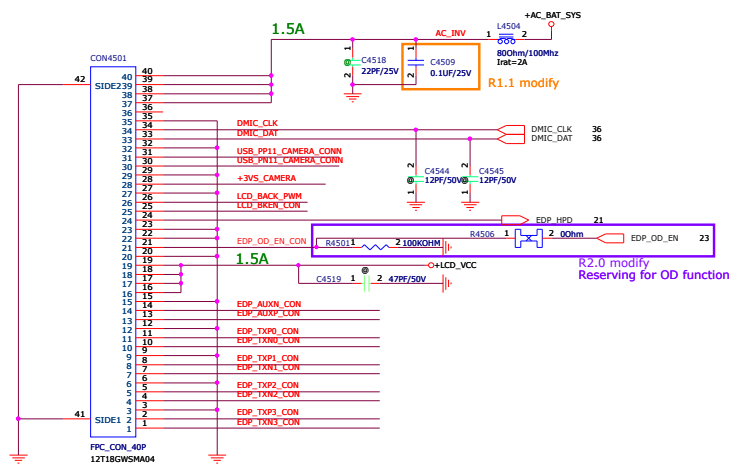


+3VS    +3VS    7,16,21,22,23,24,28,30,31,32,33,36,45,48,50,51,57,74,87,88,89,91,92,96  
+3VSUS    +3VSUS    7,21,22,23,24,26,28,30,31,33,36,48,51,53,68,74,81,88,92,96  
+3VM\_SPD    +3VM\_SPI    28

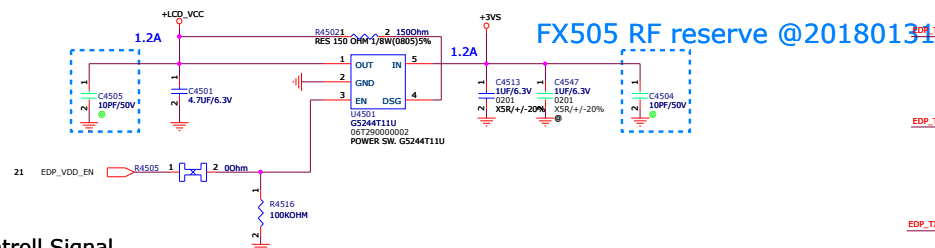




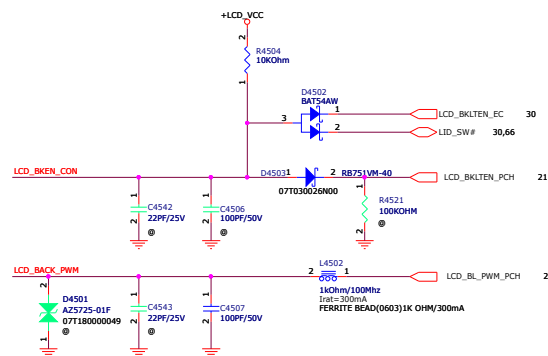
## eDP Conn.



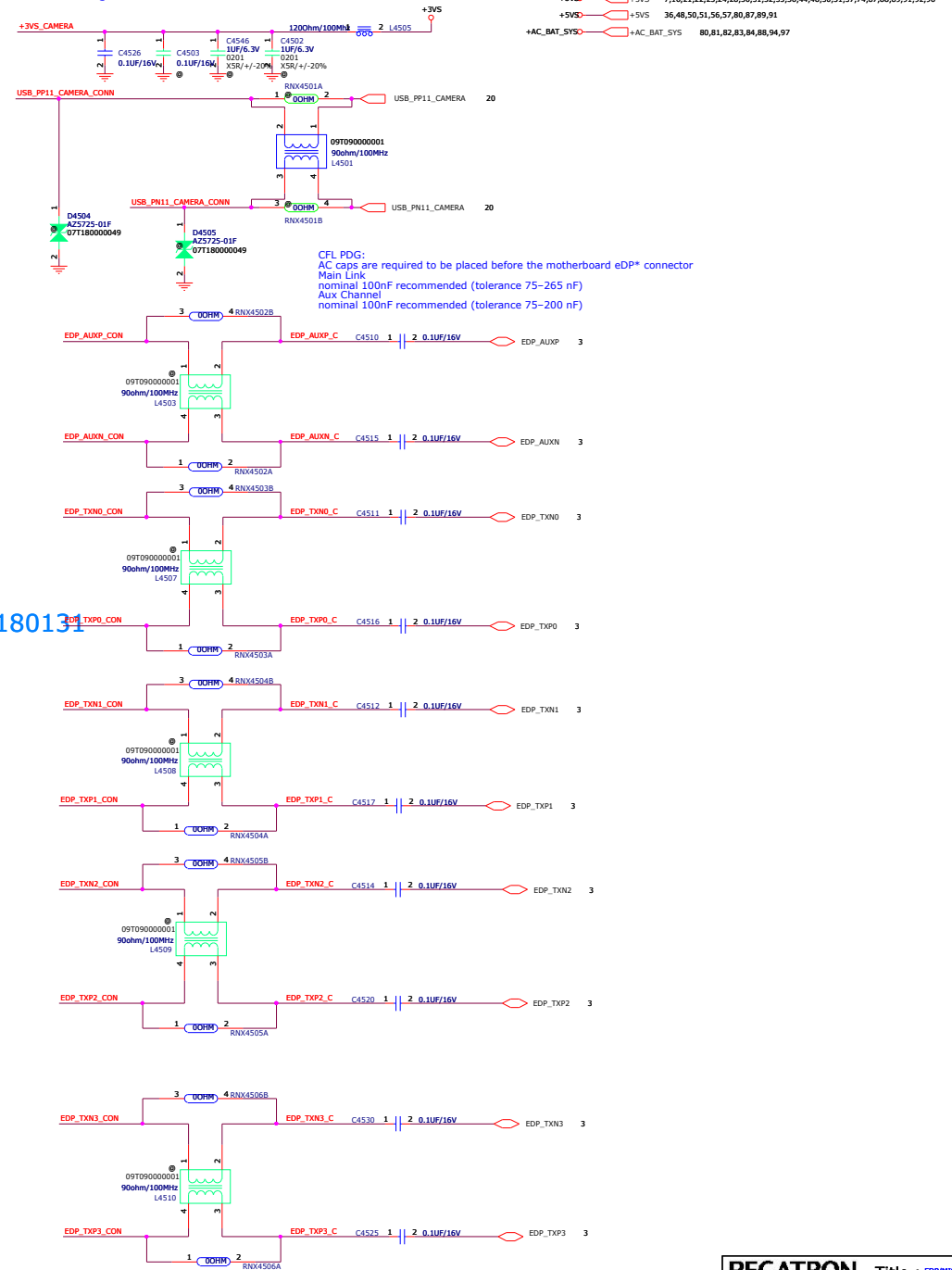
LCD VDDEN / +LED\_VCC



## Control Signal

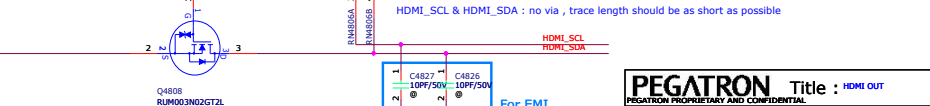
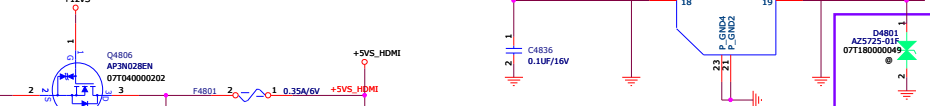
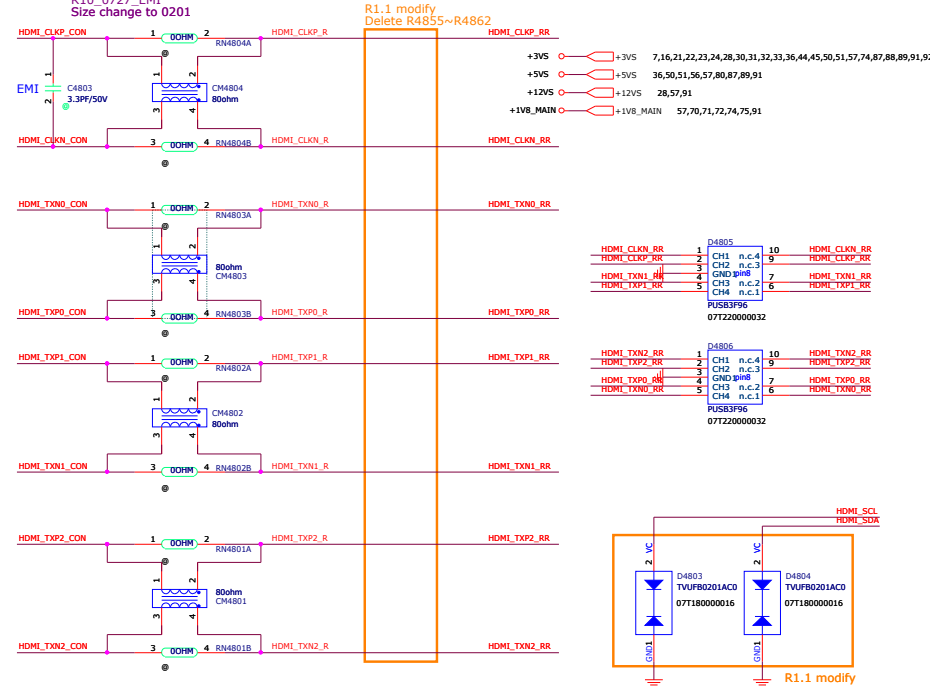
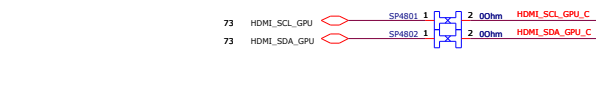
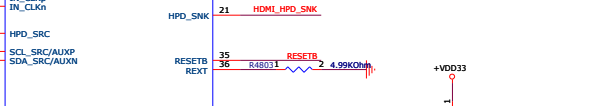
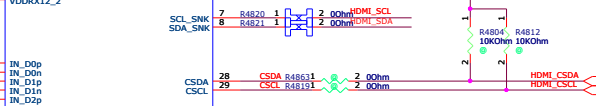
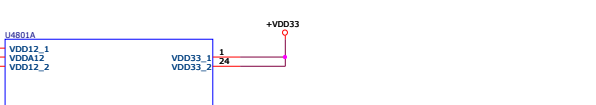
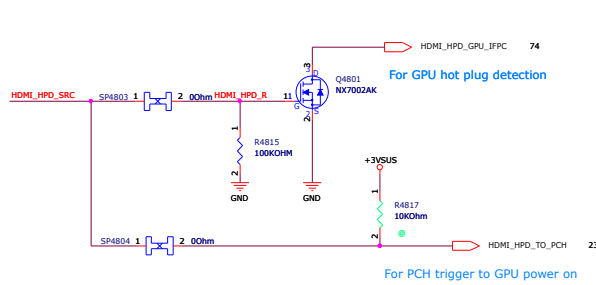
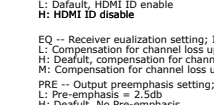
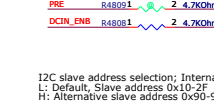
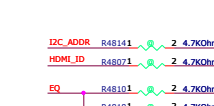
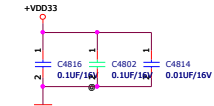
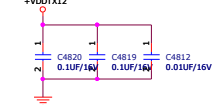
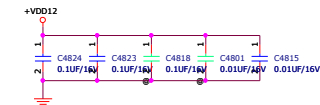
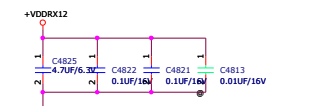
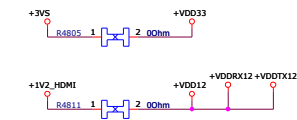
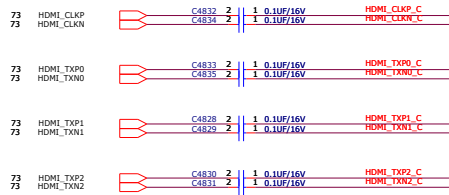


Camera Signal





# HDMI



I2C slave address selection; Internal pull down  
L: Default, Slave address 0x10-2F  
H: Alternative slave address 0x90-9F; 0xD0-DF

HDMI ID enable; Internal pull down  
L: Default, HDMI ID enable  
H: HDMI ID disable

EQ -- Receiver equalization setting; Internal pull up  
L: Compensation for channel loss up to 13db  
H: Default, compensation for channel loss up to 17db

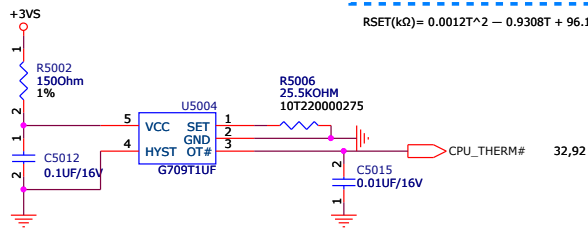
PRE -- Output preemphasis setting; Internal pull up  
L: Pre-emphasis = 2.5db  
H: Default, No Pre-emphasis



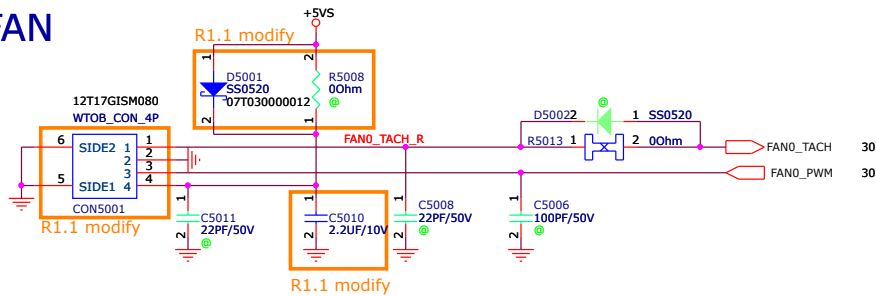
CPU Thermal Sensor

temperature set=85 C

$RSET(k\Omega) = 0.0012T^2 - 0.9308T + 96.147$

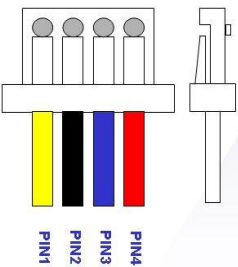


CPU FAN



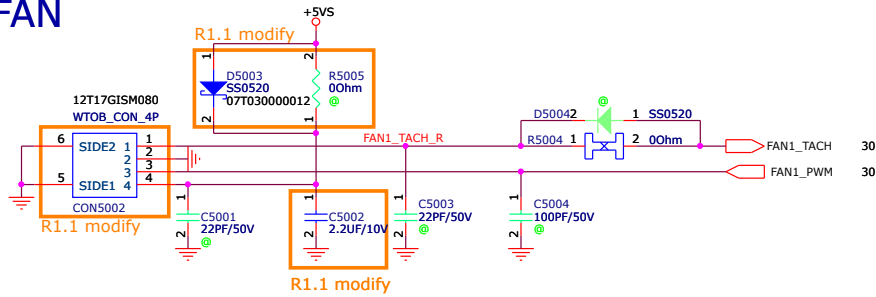
EC(PU@+3VS,10Kohm

4Pins Fan Connector Pins Definition



Pin No.	Function
Pin 1	TACHO
Pin 2	GNA
Pin 3	PWM
Pin 4	+5V

GPU FAN



EC(PU@+3VS,10Kohm

PEGATRON Title : FAN/THERMAL

PEGATRON PROPRIETARY AND CONFIDENTIAL  
BG1-HW RDC-HW2-HW RD Dept.1 Engineer: XMAN

Size A3 Project Name FX505GT  
Date: Friday, March 29, 2019 50 99 Rev 1.0

Sheet of



M.2 2280 KEY-M

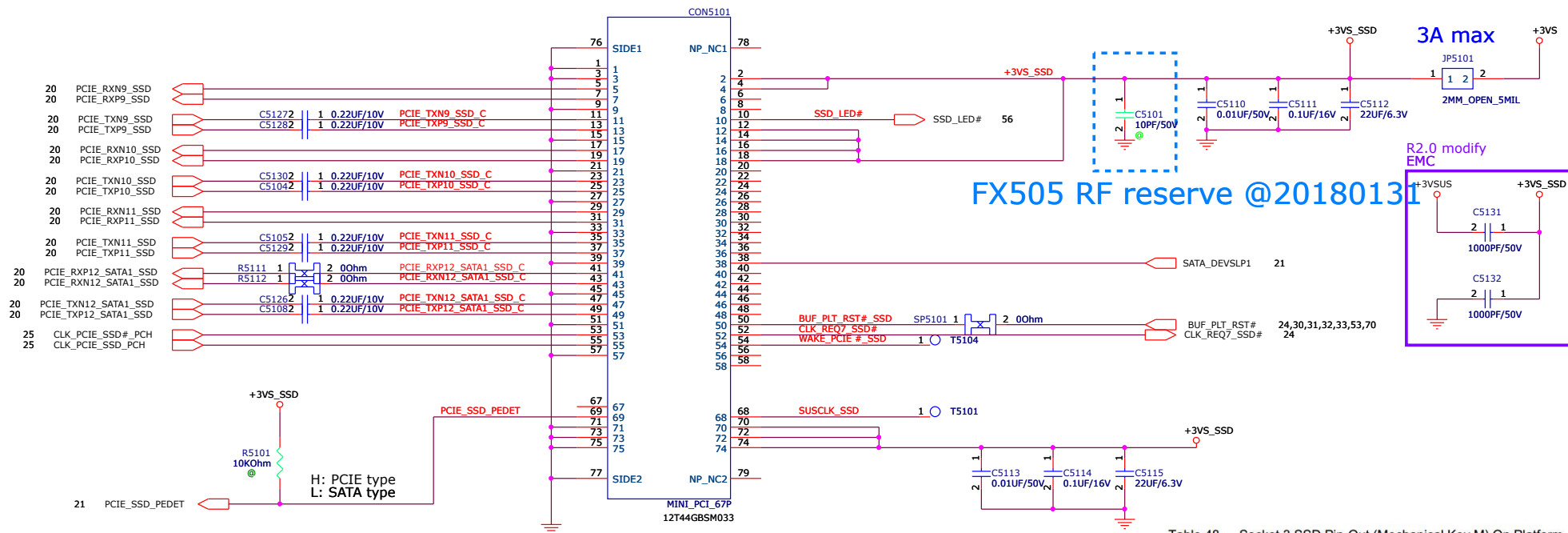
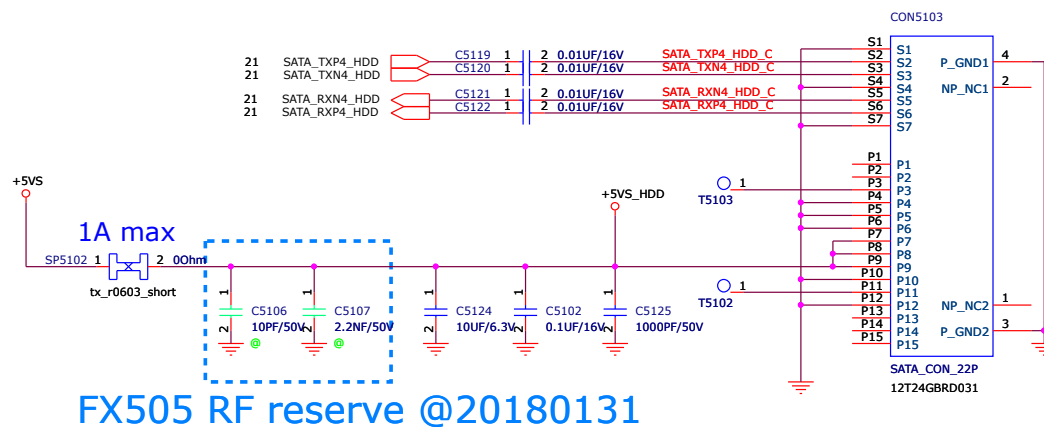


Table 48. Socket 3 SSD Pin-Out (Mechanical Key M) On Platform

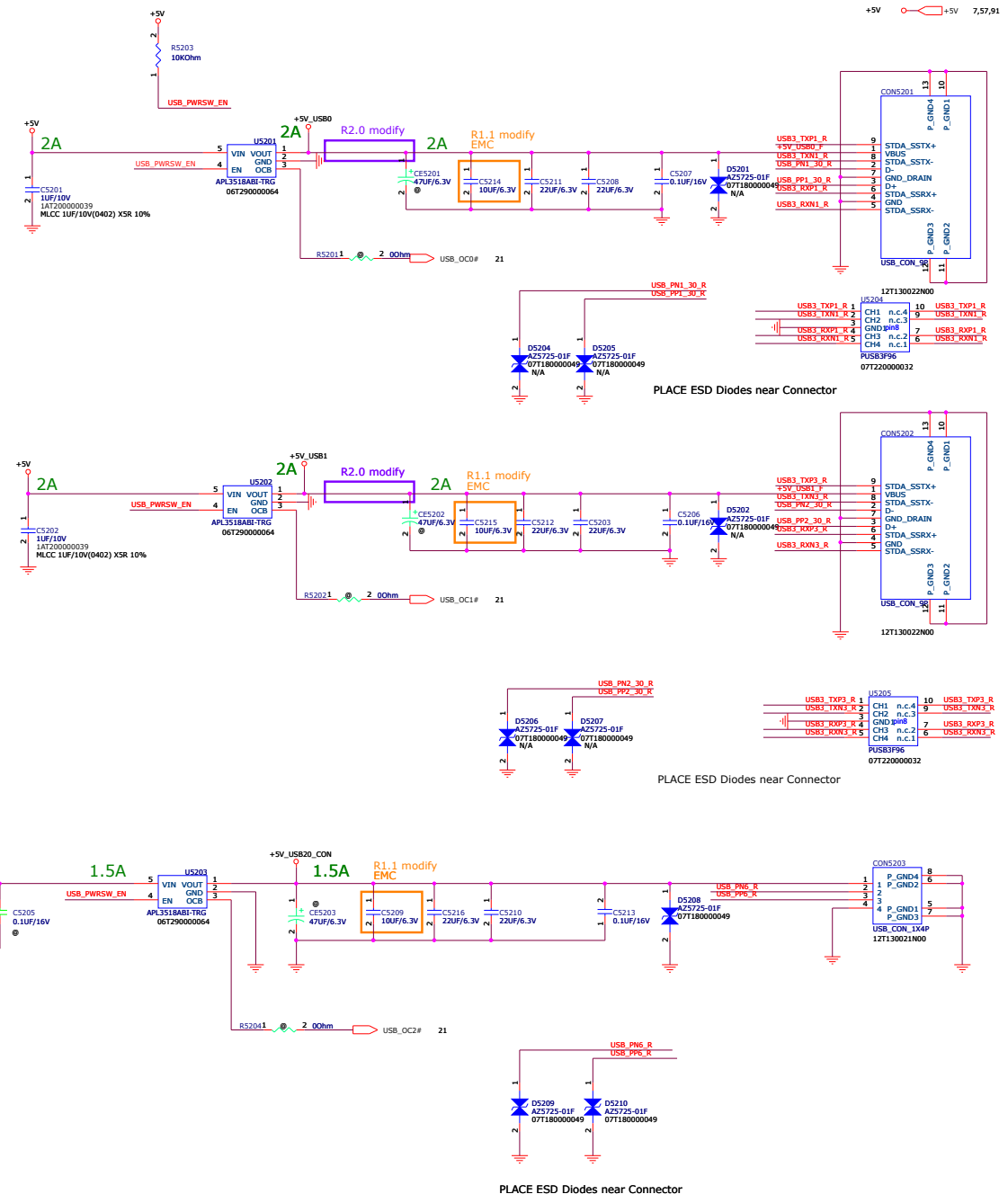
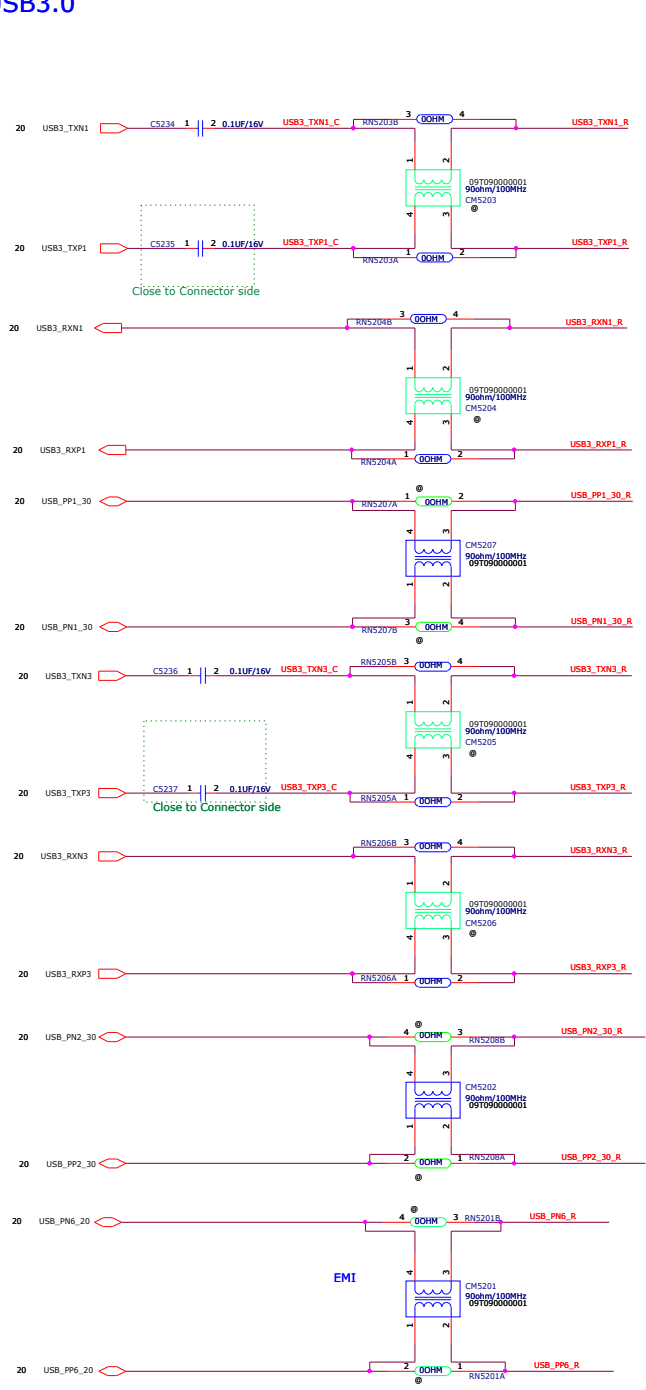
74	3.3V	GND	7
72	3.3V	GND	7
72	3.3V	GND	7
68	SUSCLK(32kHz) (IO[0]/3.3V)	PEDET (NC-PCIe/GND-SATA)	6
	Connector Key	N/C	6
	Connector Key	Connector Key	
	Connector Key	Connector Key	
	Connector Key	Connector Key	
58	N/C	GND	5
54	N/C	REFCLKp	5
54	PEWAKE (I/O[0]/3.3V) or N/C	REFCLKn	5
52	CLKREQ (I/O[0]/3.3V) or N/C	GND	5
50	PERST# (IO[0]/3.3V) or N/C	GND	5
48	N/C	PTPtoSATA-A+	4
46	N/C	PTPtoSATA-A-	4
44	N/C	GND	4
42	N/C	PERtoSATA-B	4
40	N/C	PERtoSATA-B+	4
38	DEVSLP (I/O)	GND	3
36	N/C	PTP1+	3
34	N/C	PTP1-	3
32	N/C	GND	3
30	N/C	PERp1+	3
28	N/C	PERn1-	2
26	N/C	GND	2
24	N/C	PTP2+	2
22	N/C	PTP2-	2
20	N/C	GND	2
18	3.3V	PERp2+	1
16	3.3V	PERn2-	1
14	3.3V	GND	1
12	3.3V	PTP3+	1
10	DAS/DS# (I/O)/LED#1 (I/O)/3.3V	PTP3-	1
8	N/C	GND	1
6	N/C	PERp3+	1
4	3.3V	PERn3-	1
2	3.3V	GND	1

SATA Conn. 2.5"HDD

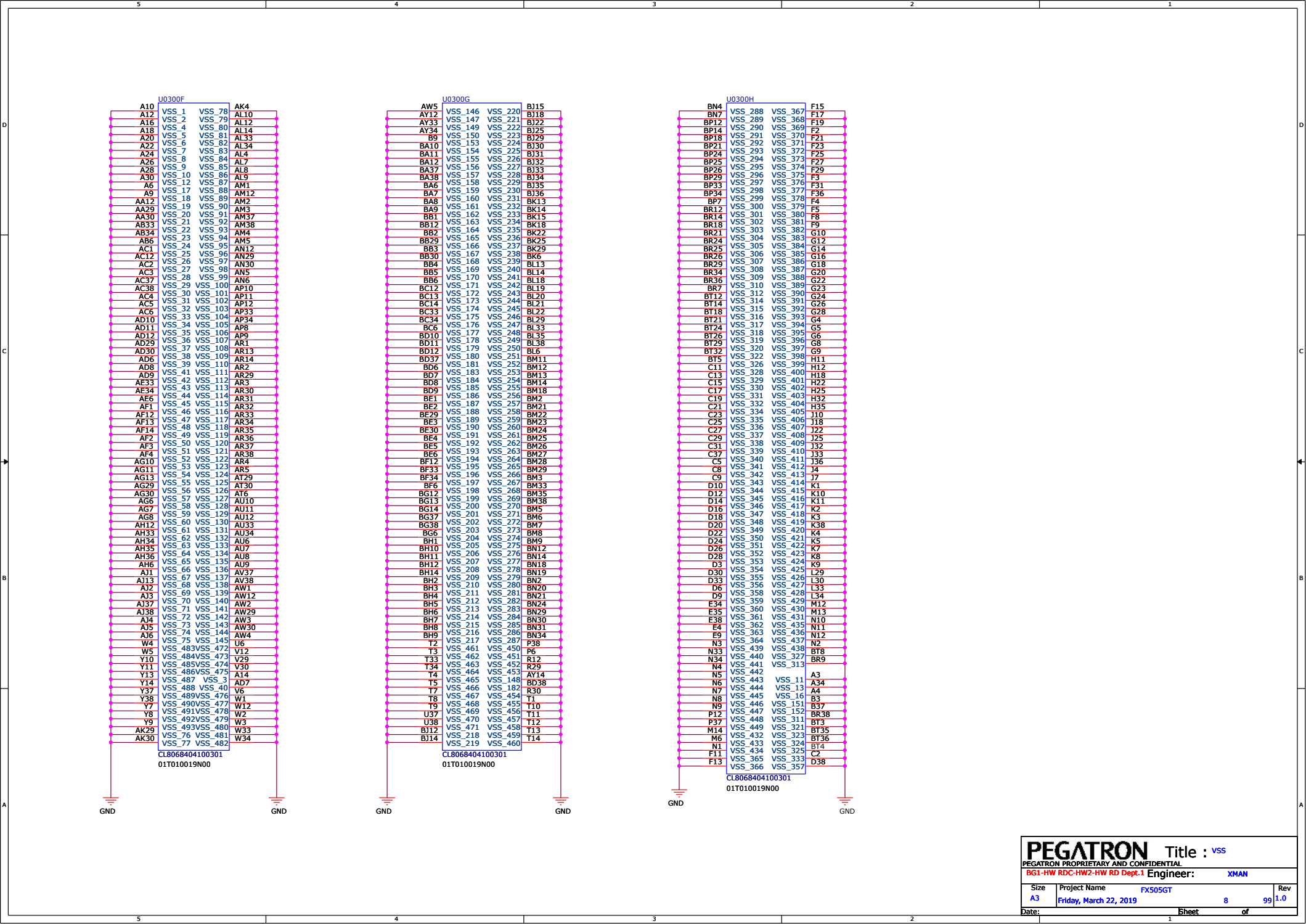




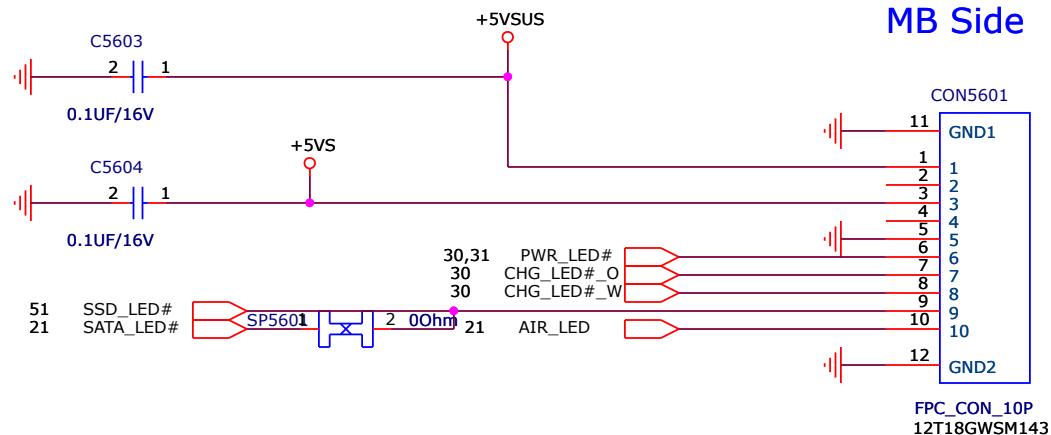
## 52.USB3.0











+5VSUS 31,81  
+5VS 36,48,50,51,57,80,87,89,91

Power LED

AIR PLANE LED

NOTE: AIR\_LED#\_R  
High -> airplane mode ON -> LED ON  
Low -> airplane mode OFF -> LED OFF

Charger LED

PCB/ID LOCATION

PWR LED  
LED5601

Charger LED  
LED5606

HDD LED  
LED5604

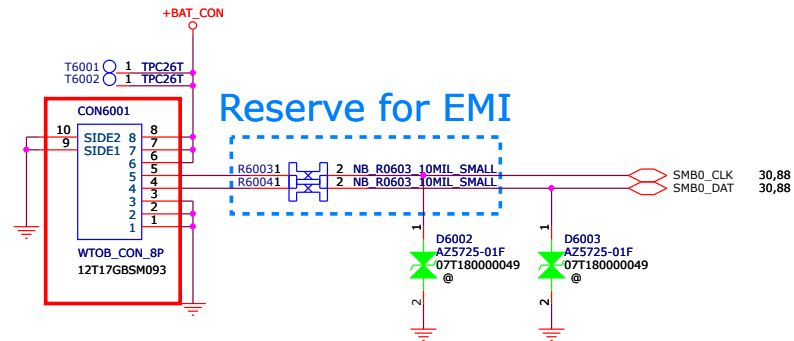
RF LED  
LED5602

HDD LED

<b>PEGATRON</b>		Title : LED	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1-HW RDC-HW2-HW RD Dept.		Engineer: XMAN	
Size A4	Project Name Friday, March 22, 2019	Rev 56 99	1.0
Date:		Sheet 1 of	

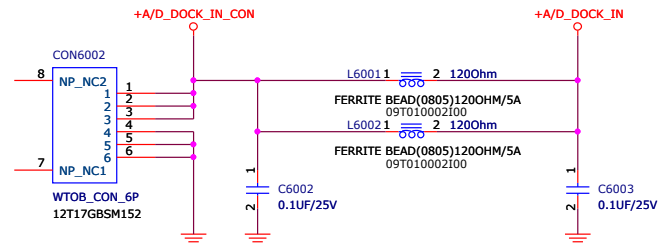


### Battery Conn.



ABBA assign: 1217-01UG0AS(1217-017L000), doesn't include 1217-01EG000 (the same pool)

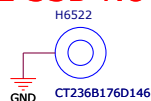
### AC in Conn.



FX505GE N17P Adaptor: 120W  
FX505GM N17E Adaptor: 150W

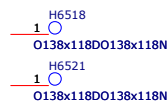


## M.2 SSD NUT:



## Tooling hole

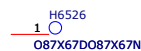
drill 3\*3.5



### drill 1.7

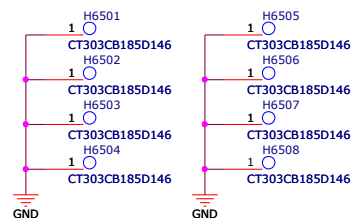


drill 2.2\*1.7

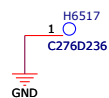


## Screw hole

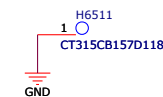
B group:  
CPU GPU bracket hole



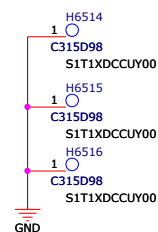
E:  
TOP: phi 7 drill 6  
BOT: phi 7 drill 6



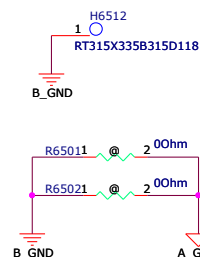
F:  
TOP: phi 8 drill 3  
BOT: phi 4 drill 3



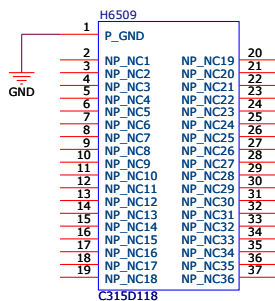
C group:  
TOP: phi 8 drill 2.5  
BOT: phi 8 drill 2.5



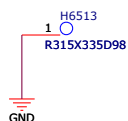
Near Audio Jack  
TOP: square 8  
BOT: phi 8 drill 3



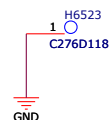
H group:



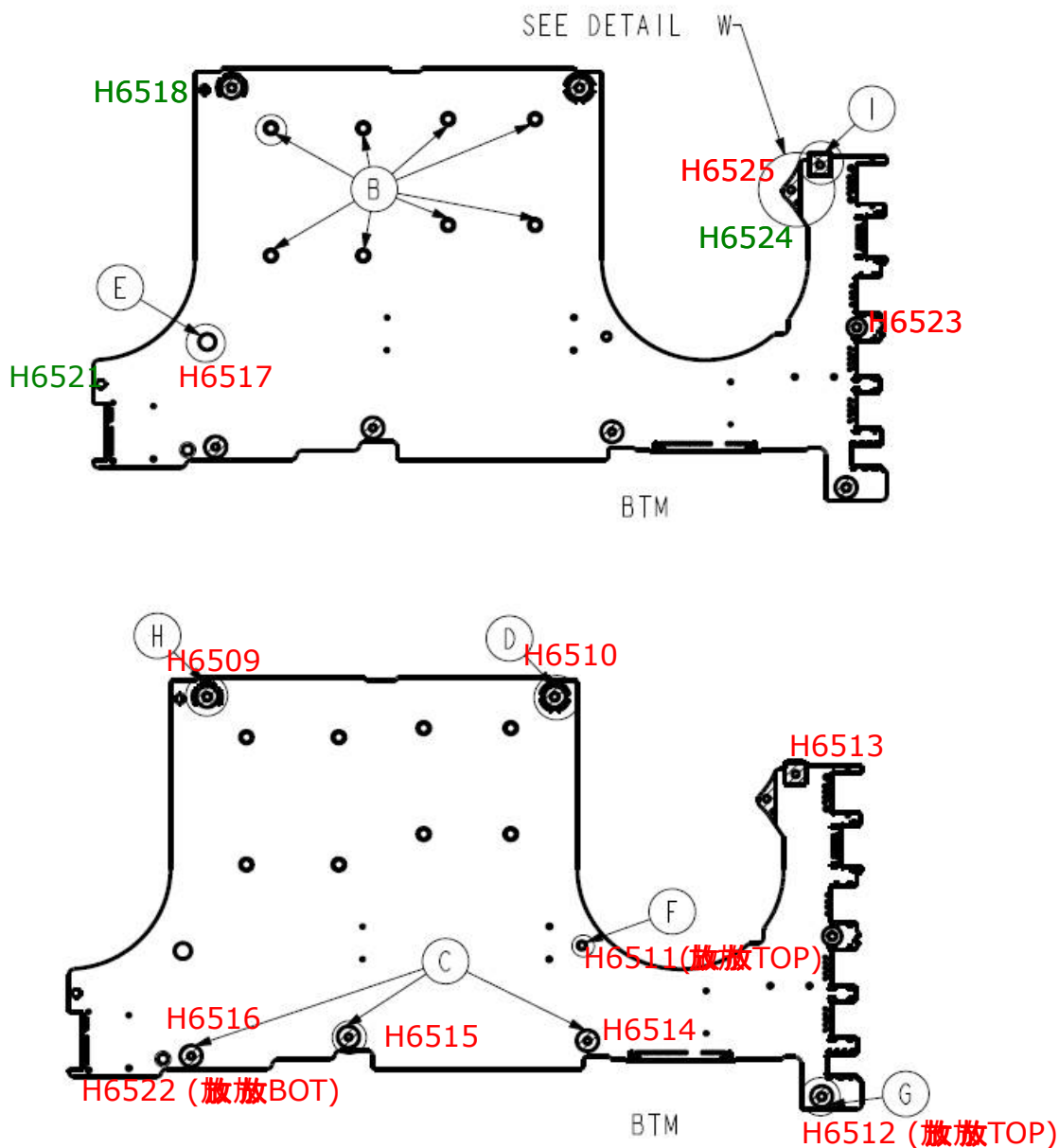
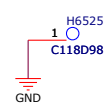
I group:  
TOP: square8\*8.5 drill 2.5  
BOT: square8\*8.5 drill 2.5



TOP: phi 7 drill 3  
BOT: phi 7 drill 3

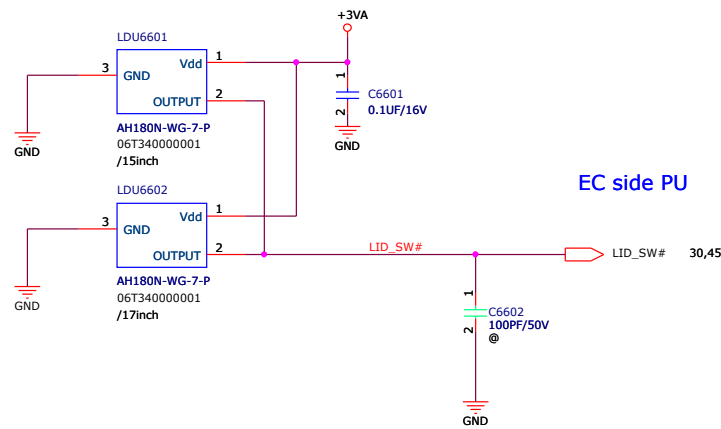


TOP: phi 3 drill 2.5  
BOT: phi 3 drill 2.5





# Hall sensor



+3VA +3VA 25,30,57,74,81,88,93,97





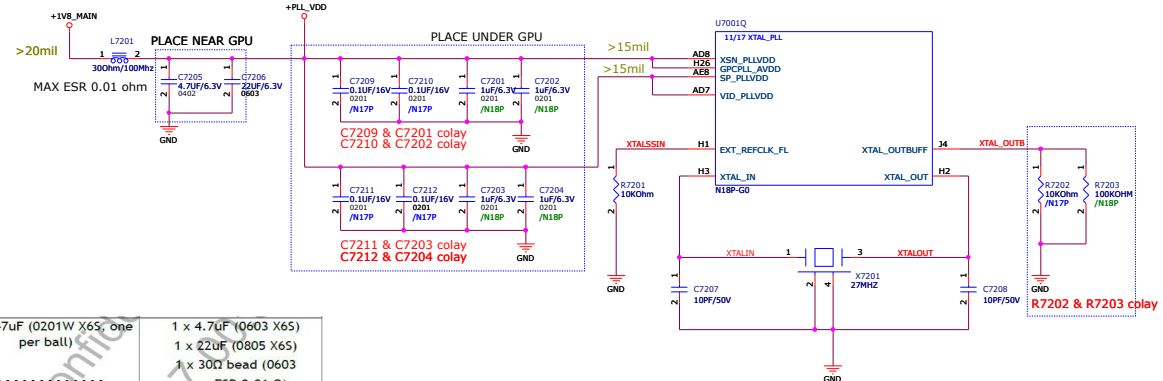


+PEX\_VDD 57,70,73,96  
+1VB\_MAIN 48,57,70,71,74,75,91  
+PLL\_VDD 73

NVIDIA (N17P)  
DA-07679-001\_v05 P.37  
-----  
XS\_PLLVDD  
Under GPU (Put at GPCPLL\_AVDD side)  
No capacitors

NVIDIA (N17P)  
DA-07679-001\_v05 P.38  
-----  
SP\_PLLVDD/VID\_PLLVDD  
Under GPU  
0.1uF x2 (0402)

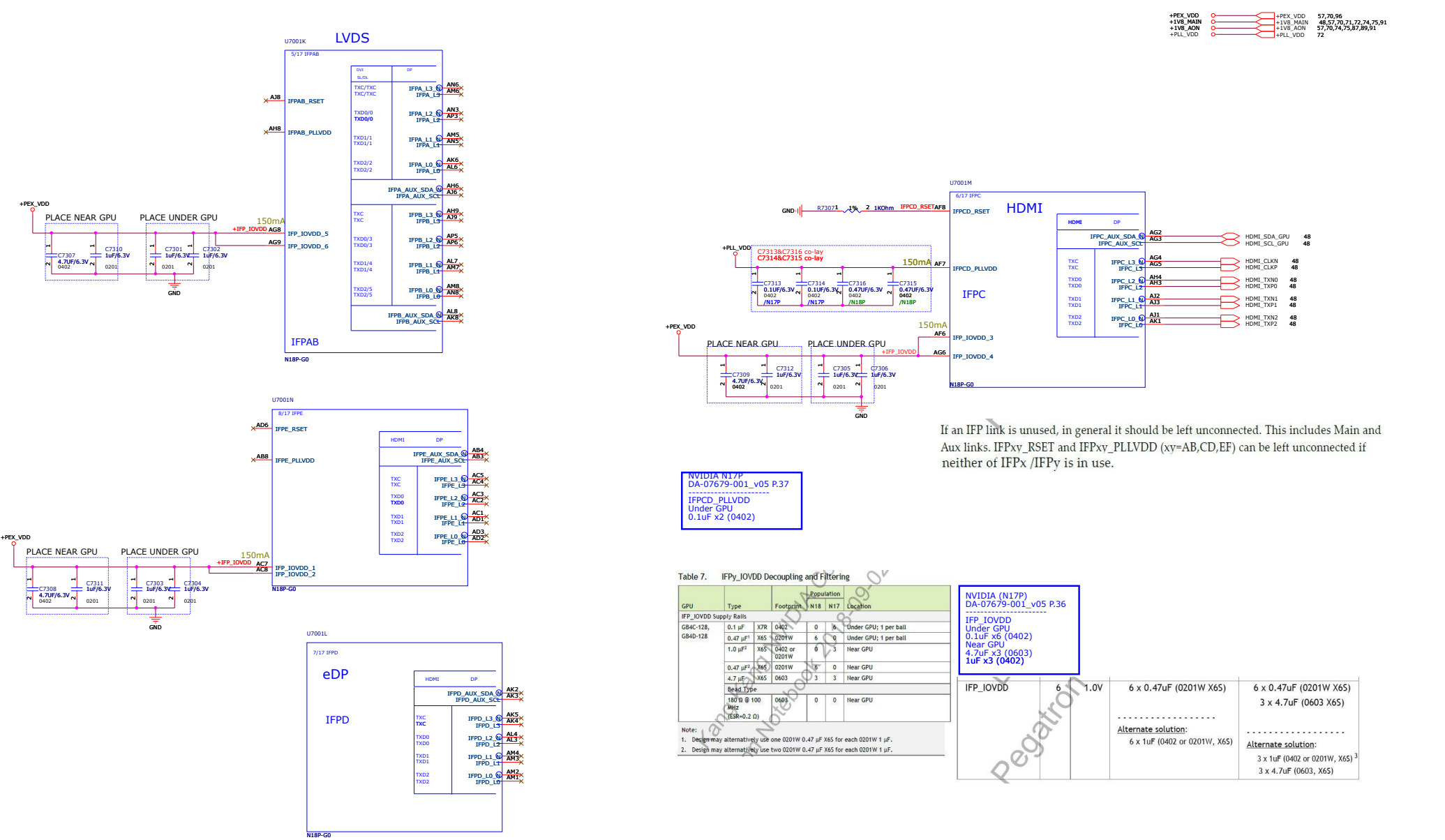
NVIDIA (N17P)  
DA-07679-001\_v05 P.38  
-----  
GPCPLL\_AVDD  
Under GPU  
0.1uF x1 (0402)  
Near GPU  
4.7uF x1 (0603)  
22 uF x1 (0805)



IFPAB_PLLVDD	1	1.8V	3 x 0.47uF (0201W X65, one per ball)	1 x 4.7uF (0603 X65)
IFPCD_PLLVDD	1			1 x 22uF (0805 X65)
IFPE_PLLVDD	1			1 x 30Ω bead (0603 max ESR 0.01 Ω)
GPCPLL_AVDDx	2		2 x 0.47uF (0201W X65)	
XS_N_PLLVDD			Alternate solution: 3 x 1uF (0402 or 0201W, X65, one per ball)	
SP_PLLVDD	1		2 x 1uF (0402 or 0201W, X65)	
VID_PLLVDD	1		1 x 0.47uF (0201W X65)	
			Alternate solution: 1 x 1uF (0402 or 0201W, X65)	
			Alternate solution: 1 x 0.47uF (0201W X65)	
			Alternate solution: 1 x 1uF (0402 or 0201W, X65)	

Part	Value	Unit	Location
IFPAB_PLLVDD	3 x 0.47uF		Under GPU
IFPCD_PLLVDD	1 x 22uF		Under GPU
IFPE_PLLVDD	1 x 30Ω bead		Under GPU
GPCPLL_AVDDx	2 x 0.47uF		Under GPU
XS_N_PLLVDD	3 x 1uF		Under GPU
SP_PLLVDD	2 x 1uF		Under GPU
VID_PLLVDD	1 x 0.47uF		Under GPU
	1 x 1uF		Under GPU
	1 x 0.47uF		Under GPU
	1 x 1uF		Under GPU





If an IFP link is unused, in general it should be left unconnected. This includes Main and Aux links. IFPxy\_RSET and IFPxy\_PLLVDD (xy=AB,CD,EF) can be left unconnected if neither of IFPx /IFPy is in use.

NVIDIA N17P  
DA-07679-001\_v05 P.37  
IFPCD\_PLLVDD  
Under GPU  
0.1uF x2 (0402)

NVIDIA (N17P)  
DA-07679-001\_v05 P.36  
IFP\_IOVDD  
Under GPU  
0.1uF x5 (0402)  
Near GPU  
4.7uF x3 (0603)  
1uF x3 (0402)

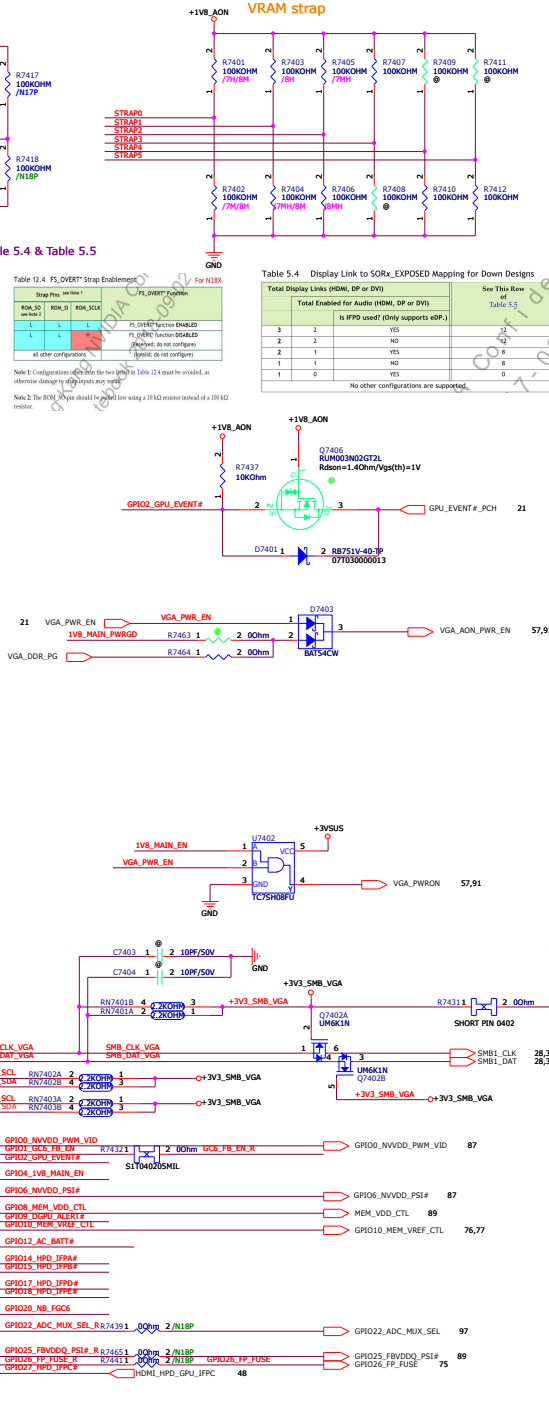
Table 7. IFPy\_IOVDD Decoupling and Filtering

GPU	Type	Footprint	N18	N17	Location
IFP_IOVDD Supply Rails					
GB4C-128,	0.1 $\mu$ F	X78	0402	0	Under GPU; 1 per ball
GB4D-128	0.47 $\mu$ F <sup>1</sup>	X85	0201W	6	Under GPU; 1 per ball
	1.0 $\mu$ F <sup>2</sup>	X85	0402 or 0201W	6	Hear GPU
	0.47 $\mu$ F <sup>2</sup>	X85	0201W	6	Hear GPU
	4.7 $\mu$ F	X85	0603	3	Hear GPU
Bezel Type					
180 $\Omega$ @ 100 MHz (ESR<0.2 $\Omega$ )	0603	0	0	0	Hear GPU

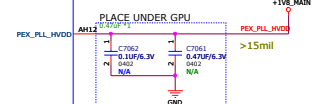
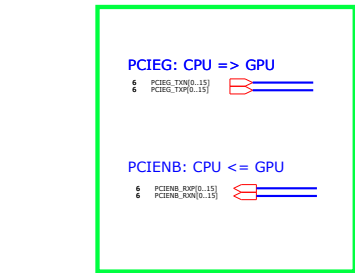
- Note:
- Design may alternatively use one 0201W 0.47  $\mu$ F X85 for each 0201W 1  $\mu$ F.
  - Design may alternatively use two 0201W 0.47  $\mu$ F X85 for each 0201W 1  $\mu$ F.

IFP_IOVDD	6	1.0V	6 x 0.47uF (0201W X65)	6 x 0.47uF (0201W X65) 3 x 4.7uF (0603 X65)
Alternate solution:		6 x 1uF (0402 or 0201W, X65)	Alternate solution: 3 x 1uF (0402 or 0201W, X65) <sup>3</sup> 3 x 4.7uF (0603, X65)	









GPU_ID	Capacitor Type	Footprint	Population		Utilization
			N18	N17	
<b>PEX_GVDD Supply Rail</b>					
GB4C-128, GB4D-128	1.0 $\mu$ F <sup>1</sup>	X65 0402 or 0201HF	0	4	Under GPU
	0.47 $\mu$ F <sup>2</sup>	X65 0603	12	0	Under GPU
	4.7 $\mu$ F	X65 0010	5	2	Hear GPU
	10 $\mu$ F	X65 0603	3	0	Under GPU
	4.7 $\mu$ F	X58 0805	0	1	Midway between GPU and power supply
	10 $\mu$ F	X65 0603	3	0	Hear GPU
	22 $\mu$ F	X58 0805	0	1	Midway between GPU and power supply
	22 $\mu$ F	X65 0805	5	0	Hear GPU
<b>PEX_HVDD Supply Rail</b>					
GB4C-128, GB4D-128	1.0 $\mu$ F <sup>1</sup>	X65 0402 or 0201HF	0	4	Under GPU
	0.47 $\mu$ F <sup>2</sup>	X65 0603	14	0	Under GPU
	4.7 $\mu$ F	X65 0010	0	2	Hear GPU
	10 $\mu$ F	X65 0603	3	0	Under GPU
	10 $\mu$ F	X58 0805	0	2	Midway between GPU and power supply
	10 $\mu$ F	X65 0805	3	0	Hear GPU
	22 $\mu$ F	X58 0805	0	1	Midway between GPU and power supply
	22 $\mu$ F	X65 0805	2	0	Hear GPU

GPU	Capacitor Type	Footprint	Population		Location
			N18	N17	
PEX_PLL_HVDD Supply Rail					
GB4C-128,	0.1 $\mu$ F	X7R	0402	0	1
GB4D-128	0.47 $\mu$ F	X6S	0201W	1	0

Note:

- Decoupling for PEX\_PLL\_HVDD is merged with PEX\_HVDD, and Design may alternatively

Rail (GPU Ball)	Balls	Voltage	Filtering under GPU	Filtering Near GPU
PEX_HVDD	14	1.8V	14 x 0.47 $\mu$ F (0201V X65) 3 x 4.7 $\mu$ F (0603 X65)  Alternate solution: 7 x 1uF (0402 or 0201V, X65) <sup>1</sup> 3 x 4.7 $\mu$ F (0603 X65)	3 x 10 $\mu$ F (0805 X65) 2 x 22 $\mu$ F (0805 X65)
PEX_DVDD	6	1.0V	12 x 0.47 $\mu$ F (0201V X65) 3 x 4.7 $\mu$ F (0603 X65)  Alternate solution: 6 x 1uF (0402 or 0201V, X65) <sup>1</sup> 3 x 4.7 $\mu$ F (0603 X65)	3 x 10 $\mu$ F (0805 X65) 2 x 22 $\mu$ F (0805 X65)



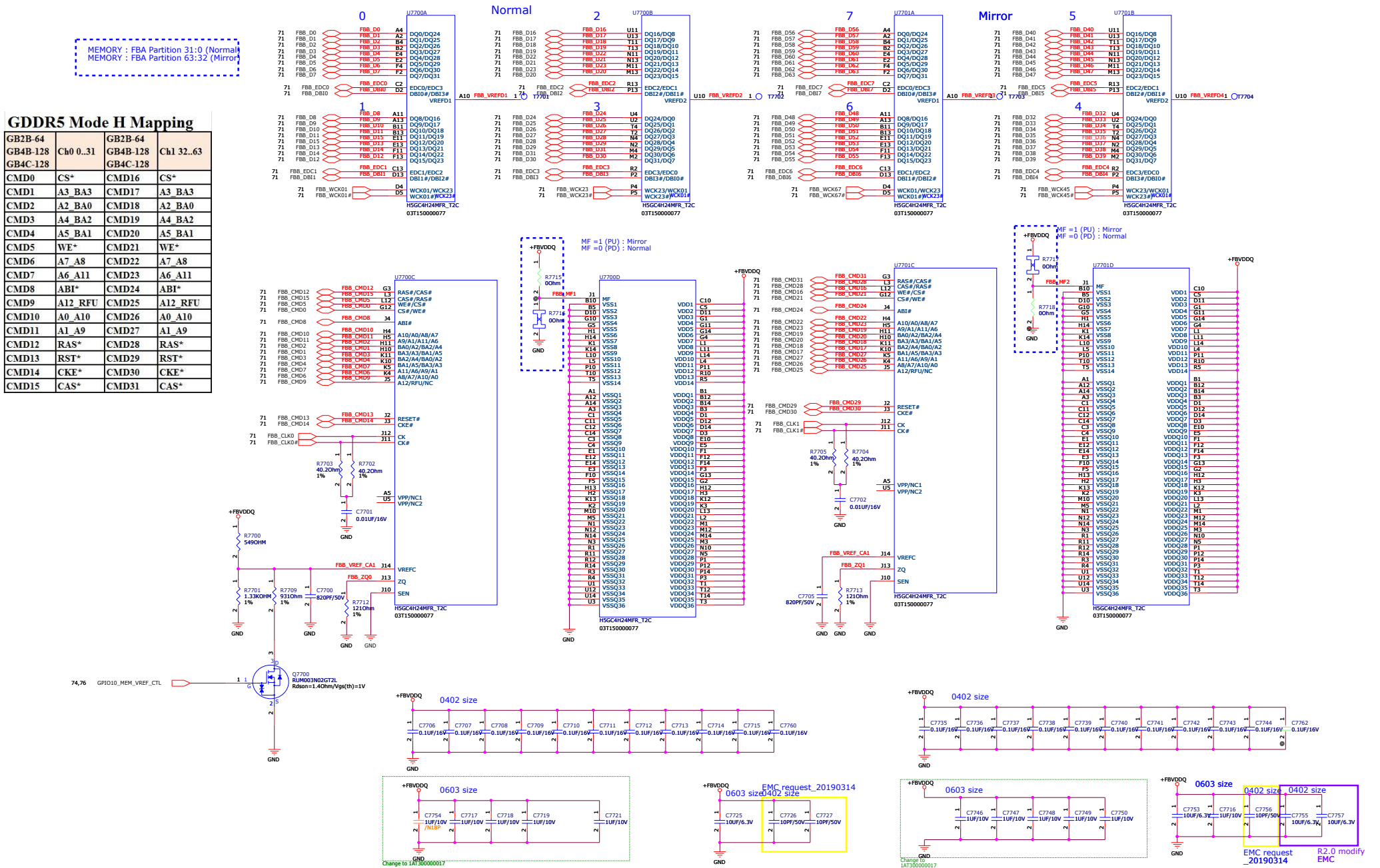
WLAN bypass capacitors:



Date: \_\_\_\_\_ Sheet: \_\_\_\_\_

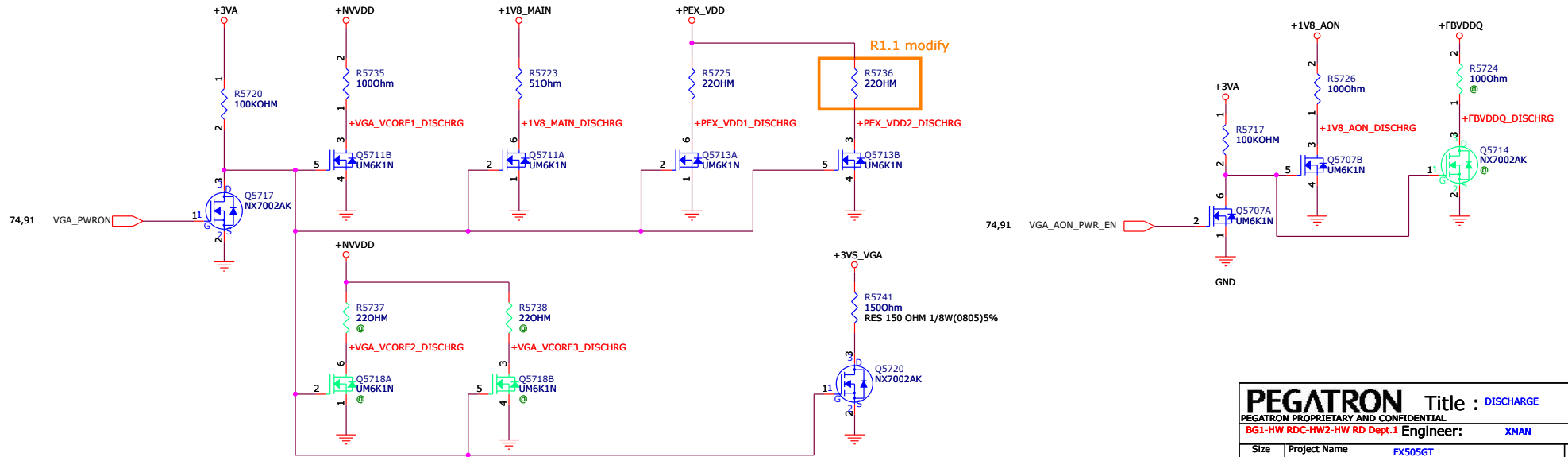
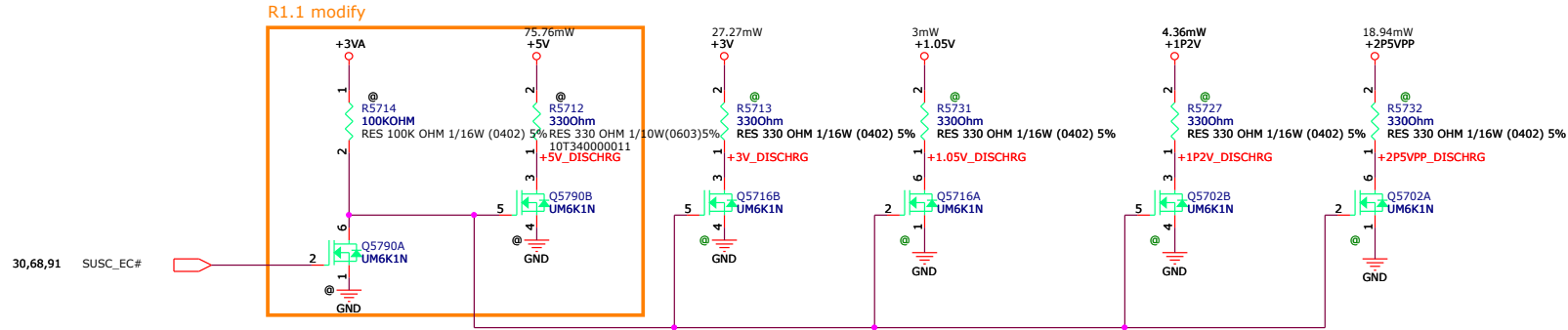
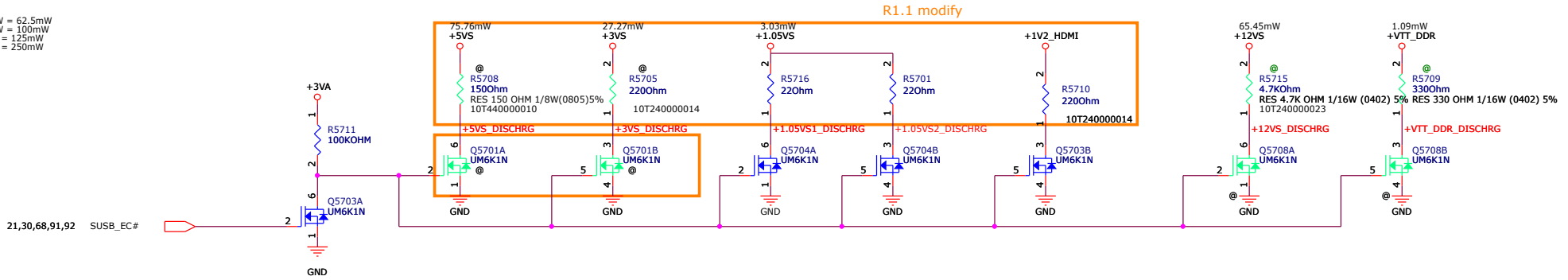


GDDR5 Mode H Mapping			
GB2B-64 GB4B-128 GB4C-128	Ch0 0..31	GB2B-64 GB4B-128 GB4C-128	Ch1 32..63
CMD0	CS*	CMD16	CS*
CMD1	A3 BA3	CMD17	A3 BA3
CMD2	A2 BA0	CMD18	A2 BA0
CMD3	A4 BA2	CMD19	A4 BA2
CMD4	A5 BA1	CMD20	A5 BA1
CMD5	WE*	CMD21	WE*
CMD6	A7 A8	CMD22	A7 A8
CMD7	A6 A11	CMD23	A6 A11
CMD8	AB1*	CMD24	AB1*
CMD9	A12 RFU	CMD25	A12 RFU
CMD10	A0 A10	CMD26	A0 A10
CMD11	A1 A9	CMD27	A1 A9
CMD12	RAS*	CMD28	RAS*
CMD13	RST*	CMD29	RST*
CMD14	CKE*	CMD30	CKE*
CMD15	CAS*	CMD31	CAS*



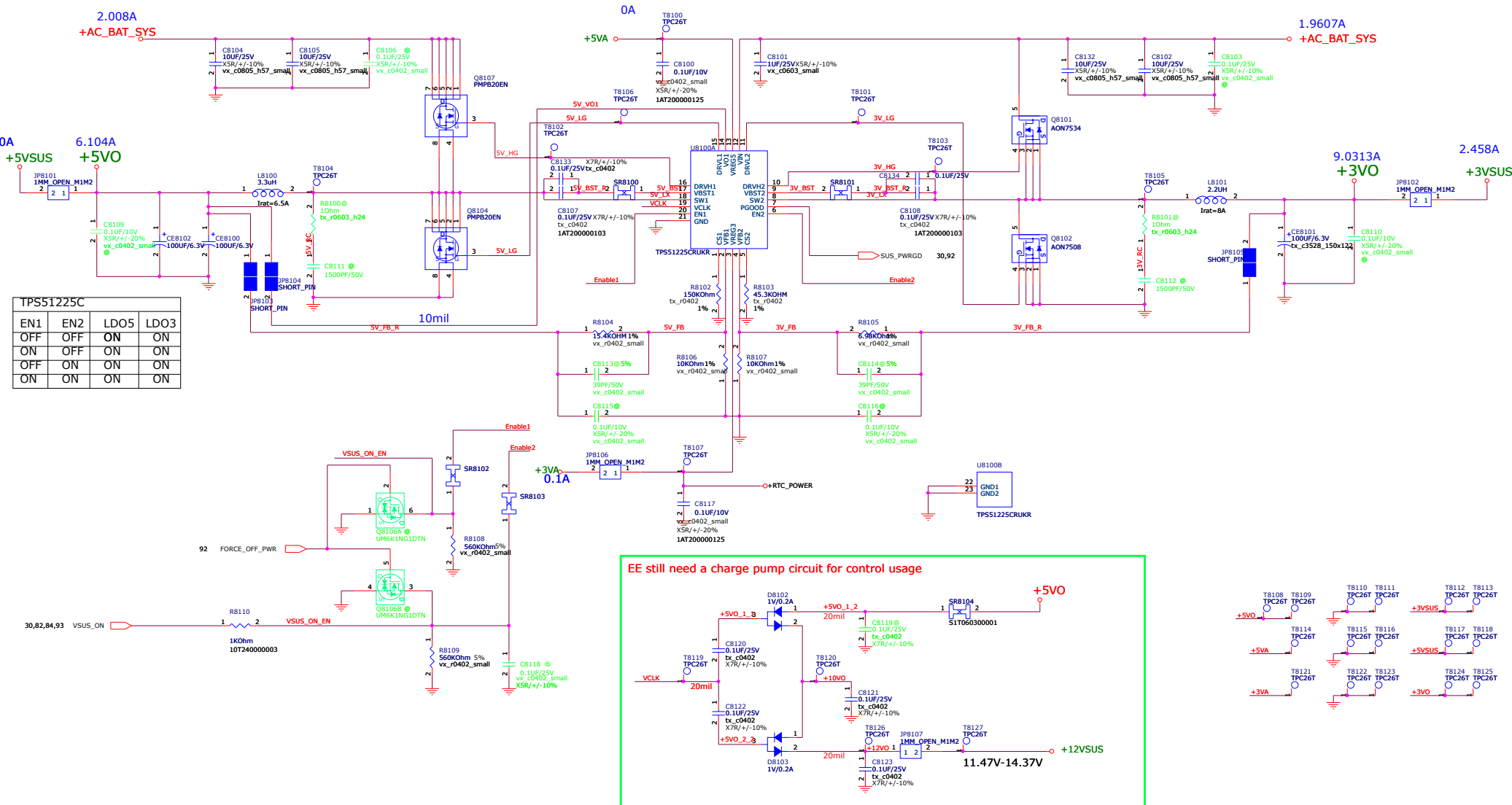


$V^2/R$   
 0402 = 1/16W = 62.5mW  
 0603 = 1/10W = 100mW  
 0805 = 1/8W = 125mW  
 1206 = 1/4W = 250mW



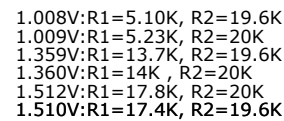


## +5V0 & +3V0 POWER SUPPLY



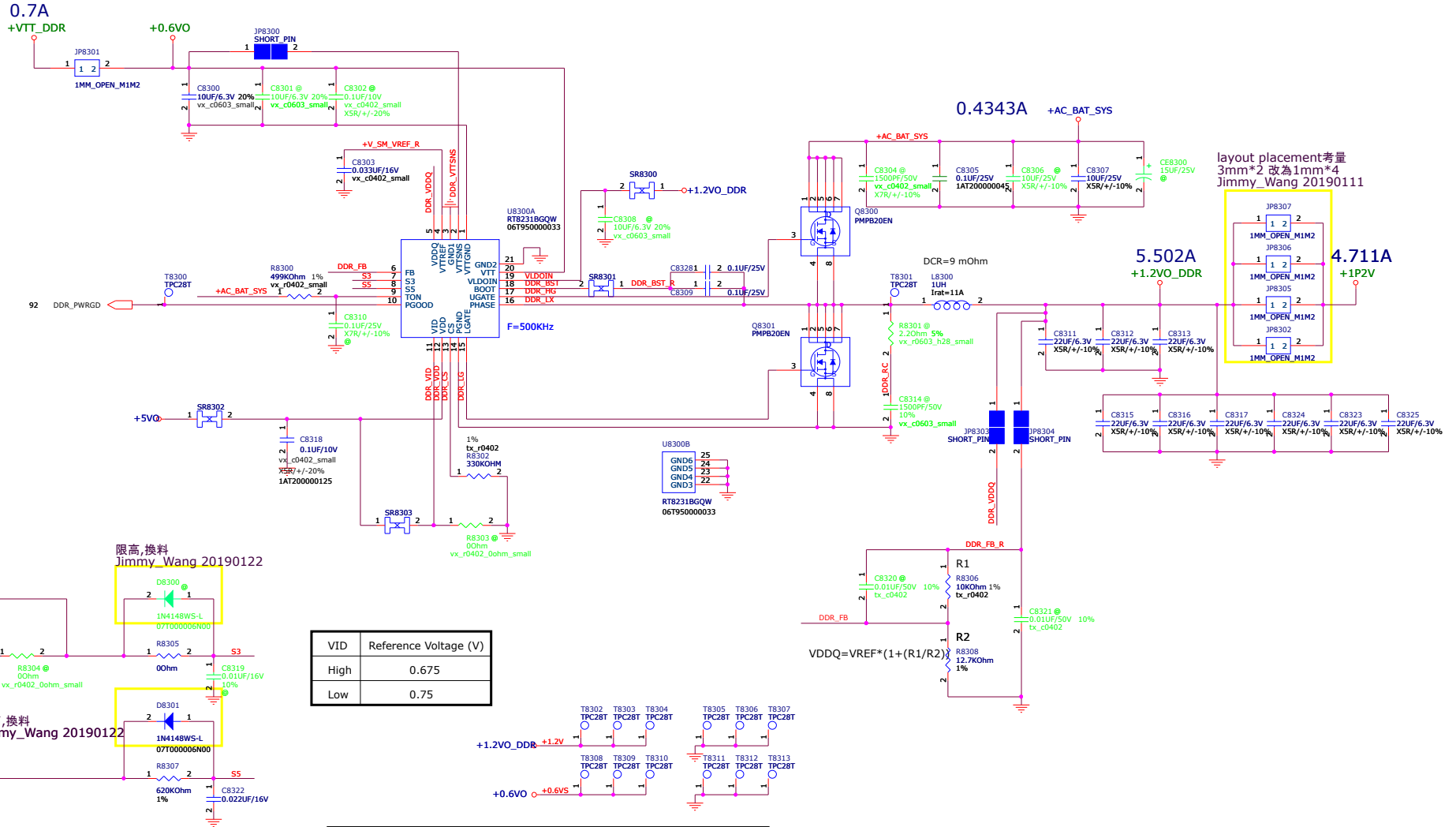


(0.3295A)





## DDR & VTT POWER SUPPLY



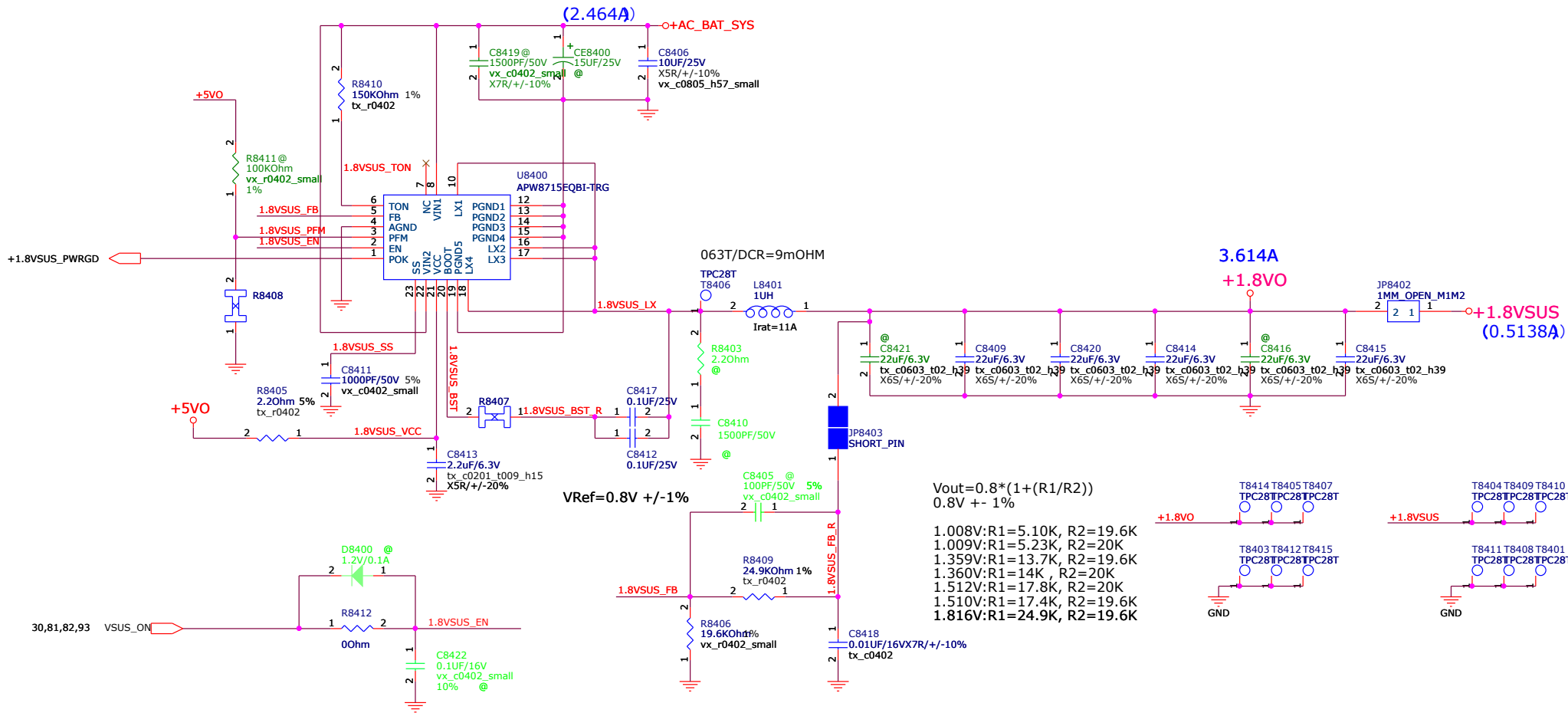
VID	Reference Voltage (V)
High	0.675
Low	0.75

SKU	Load current (A)	Low-side MOSFET (pcs)	Output 22uF/6.3V MLCC (pcs)
UMA	0 ~ 5	1	4
DSC	0 ~ 8	2	5



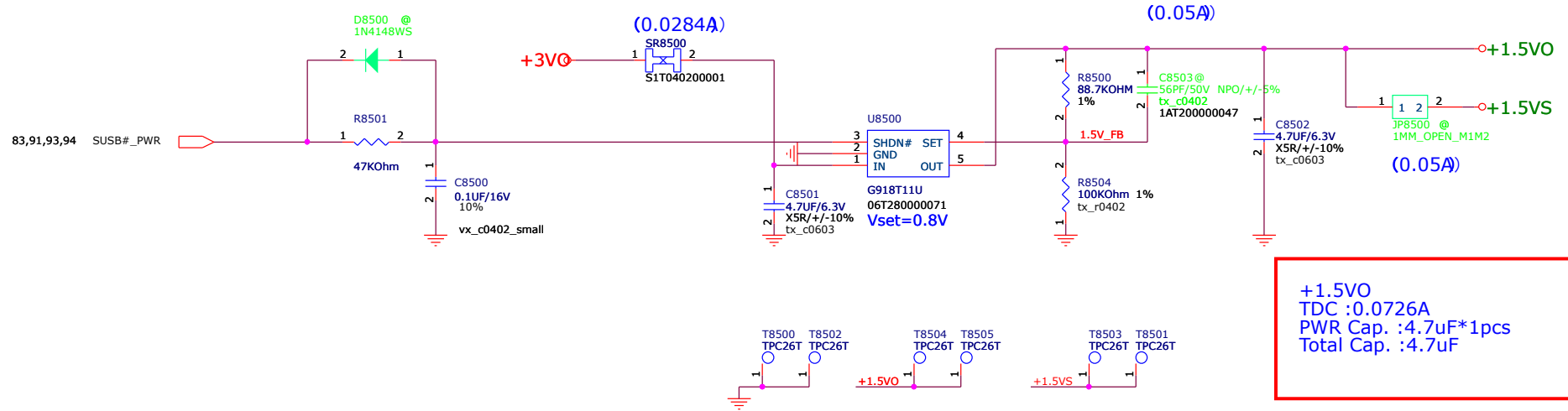
# 1.8VSUS POWER SUPPLY

換料APW8715E  
Jimmy\_Wang 20190225





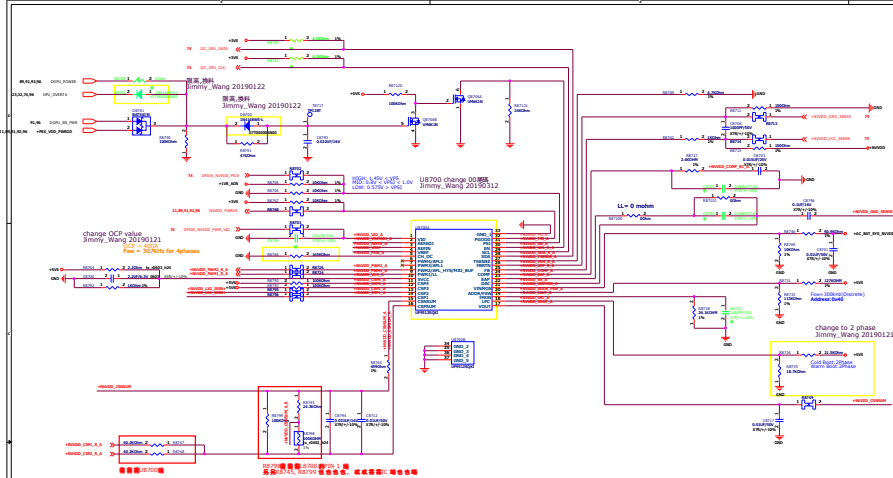
# 1.5VS POWER SUPPLY



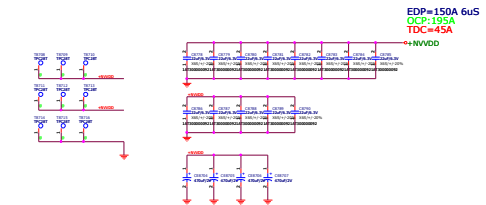
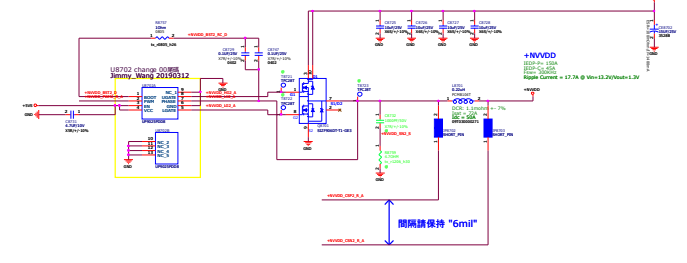
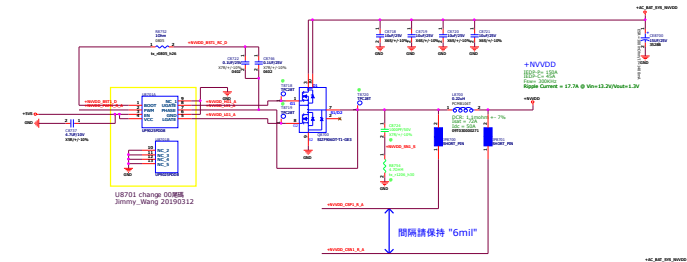
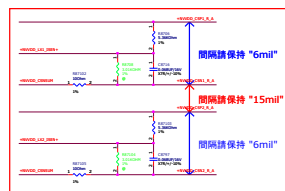






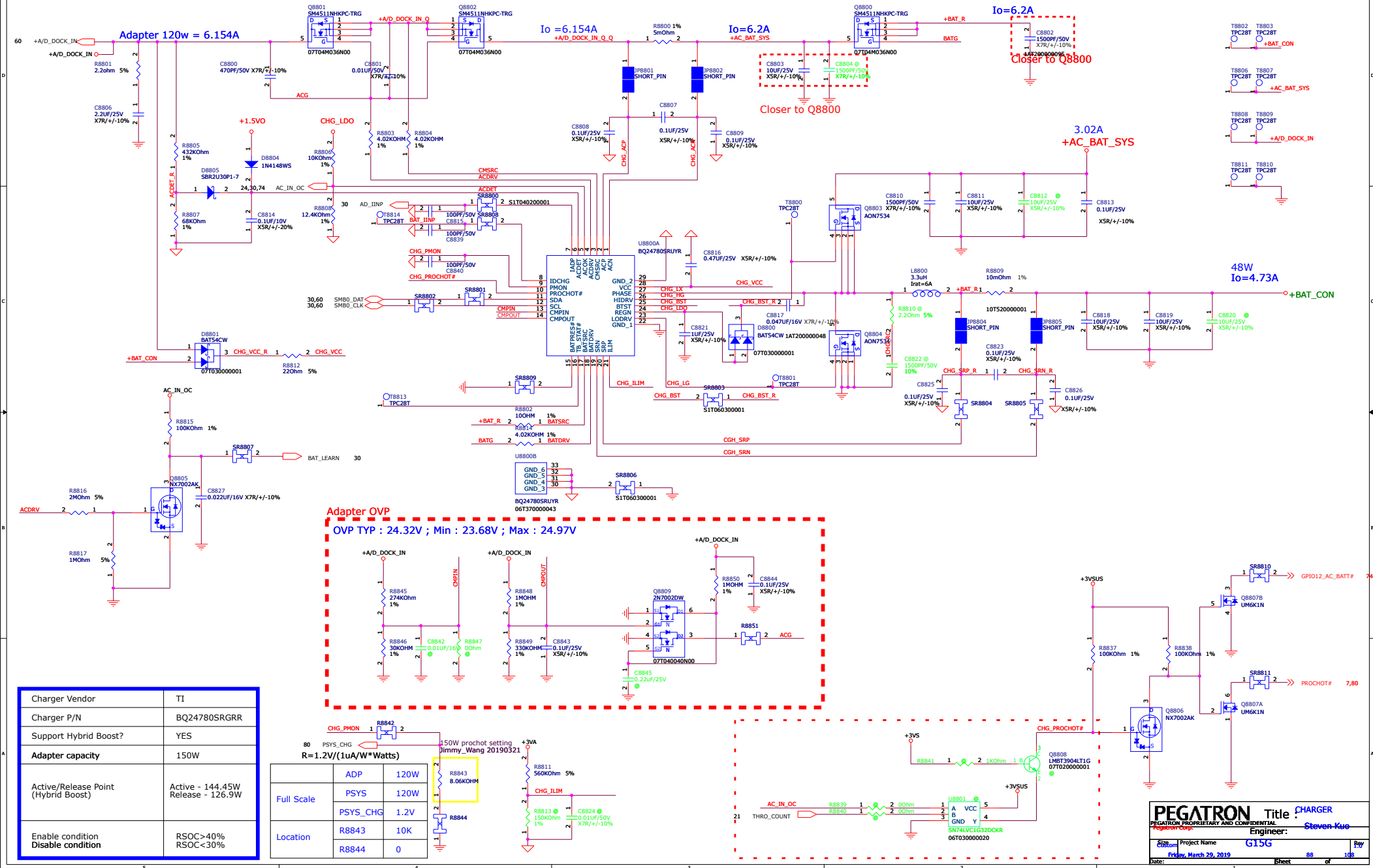


RB721	6.19K
RB718	20.3K
RB719	4.32K
RB722	16.5K
RB723	30K
CB707	4.7nF
Vmin	0.3V
Vmax	1.3V
Vboot	0.8V
VSTB	6.25mV



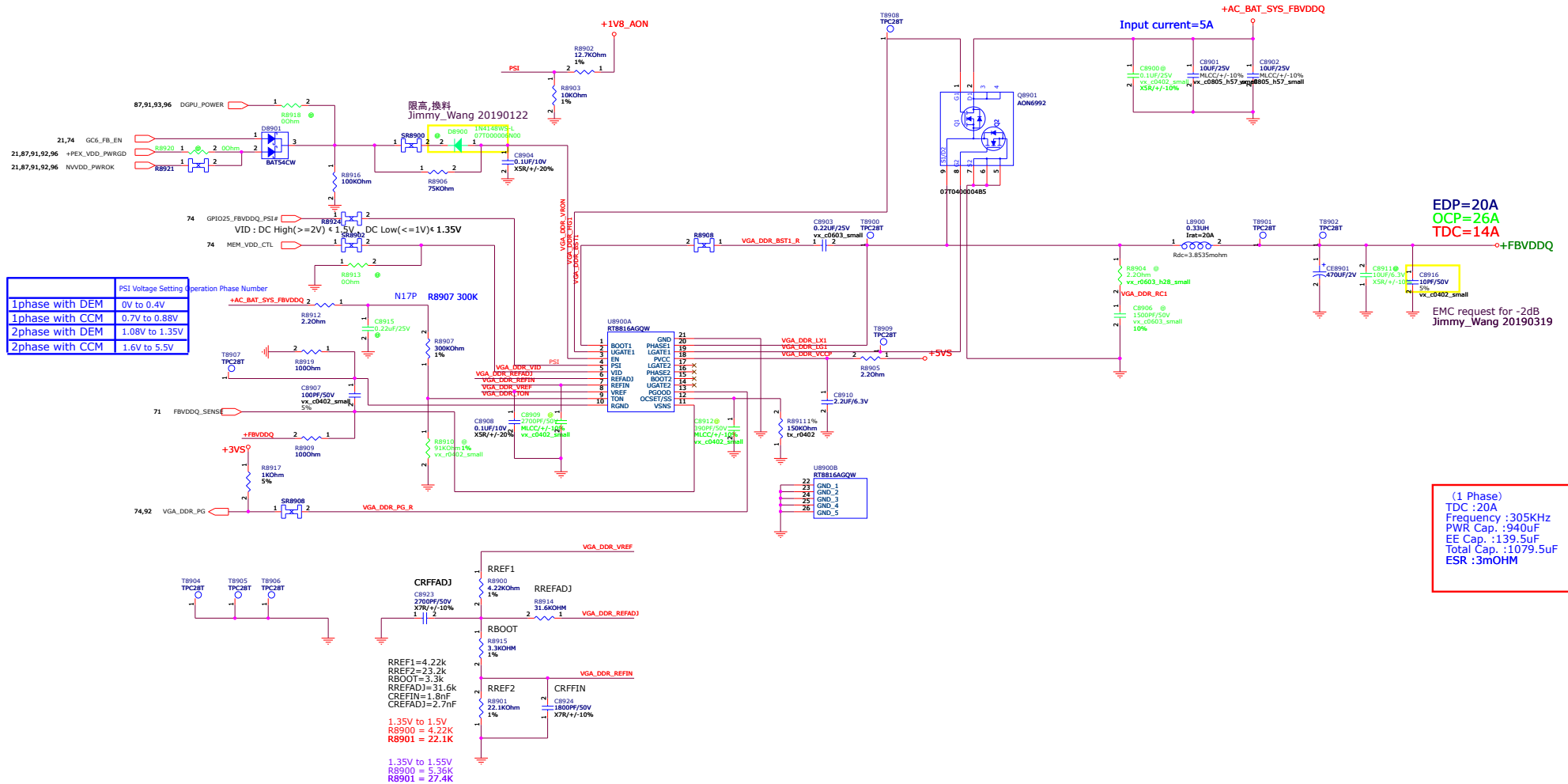


## BATTERY CHARGER





## +FBVDDQ POWER SUPPLY





D

D

C

C

B

B

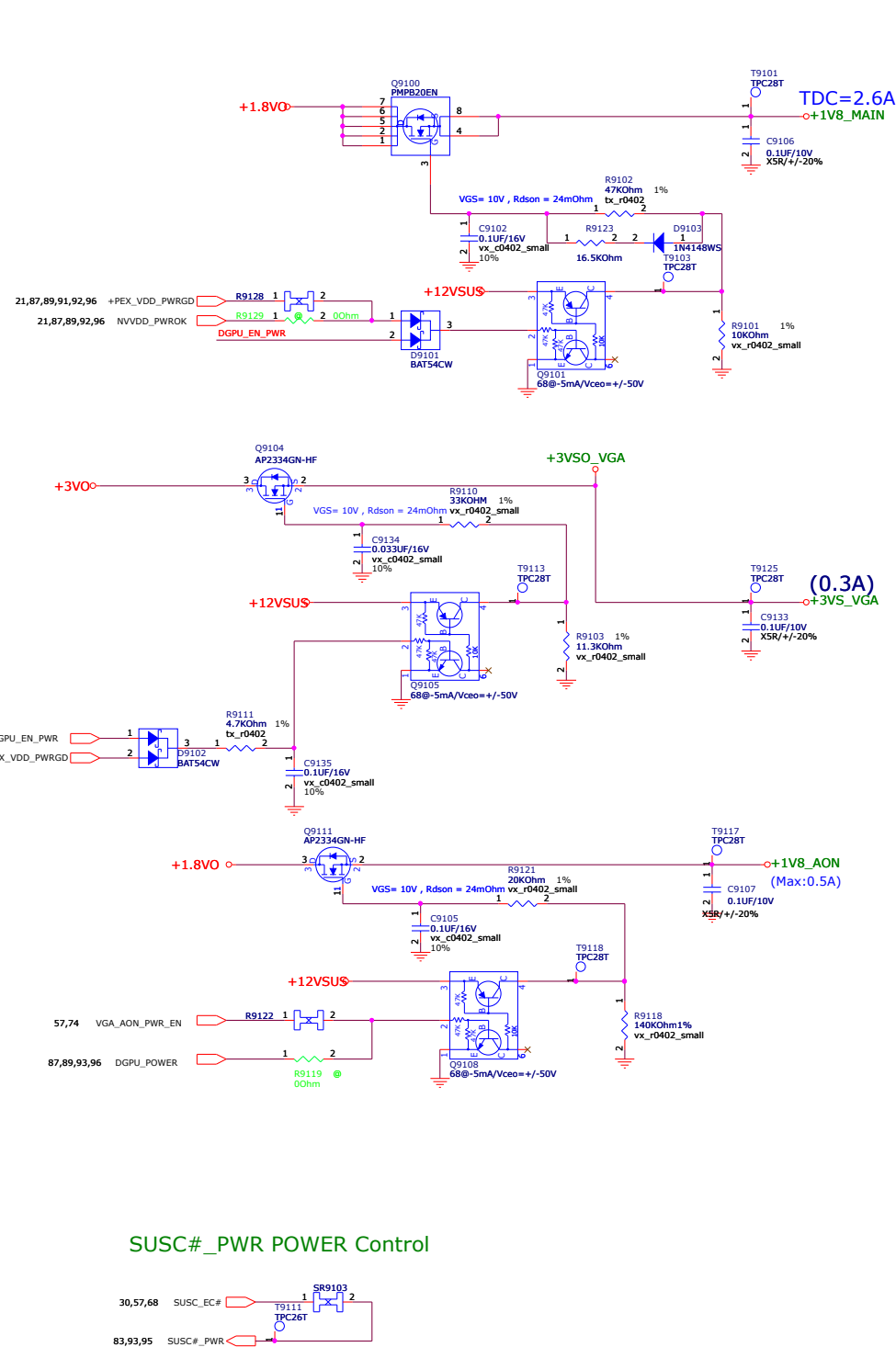
A

A

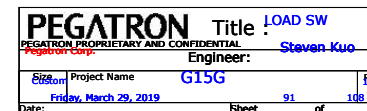
<b>PEGATRON</b>		Title . <b>DETECT</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
Size <b>Custom</b>		Engineer: <b>Steven Kuo</b>	
Project Name <b>G15G</b>		Rev <b>108</b>	
Date: <b>Friday, March 22, 2019</b>		Sheet <b>90</b> of <b>108</b>	



SUSC#	PWR	POWER
1	1	1
2	1	1
3	1	1
4	1	1
5	1	1
6	1	1
7	1	1
8	1	1
9	1	1
10	1	1
11	1	1
12	1	1
13	1	1
14	1	1
15	1	1
16	1	1
17	1	1
18	1	1
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33	1	1
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89	1	1
90	1	1
91	1	1
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96	1	1
97	1	1
98	1	1
99	1	1
100	1	1

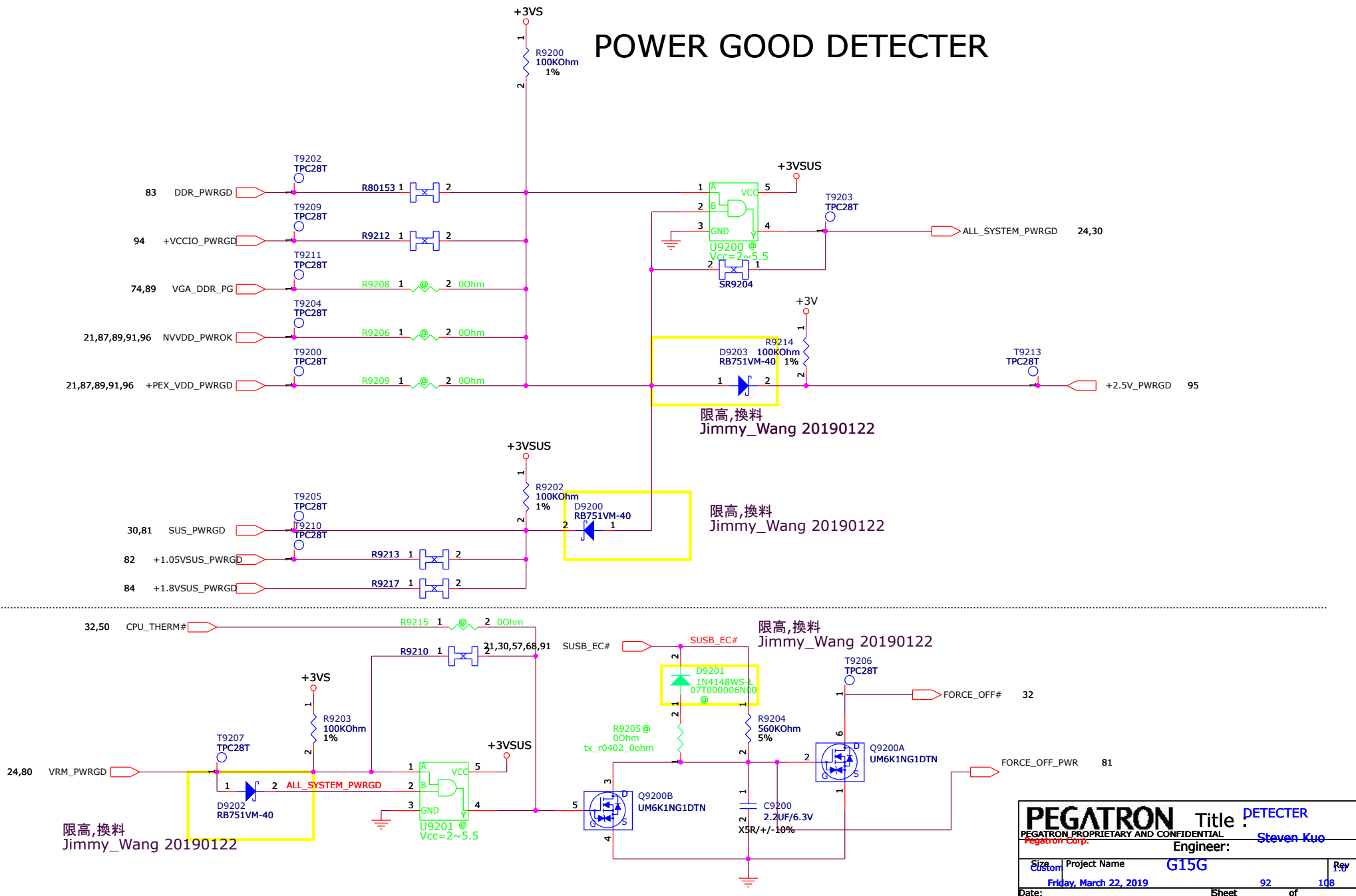


DSC\_VGA\_PWR POWER Control    SUSB#\_PWR POWER Control





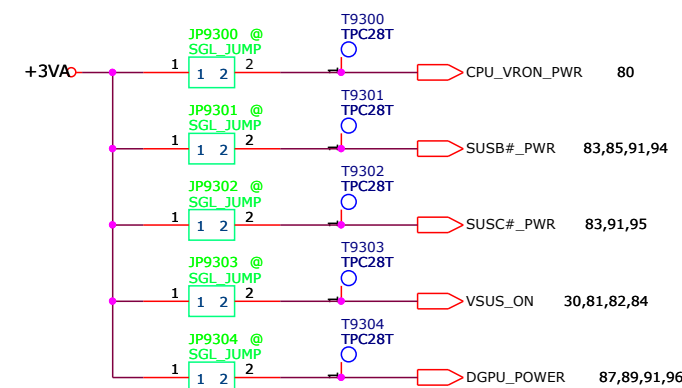
# POWER GOOD DETECTOR





+A/D_DOCK_IN		+A/D_DOCK_IN	60,88
+BAT_CON		+BAT_CON	60,88
+AC_BAT_SYS		+AC_BAT_SYS	45,80,81,82,83,84,88,94,97
+12VSUS		+12VSUS	81,91
+3VO		+3VO	81,85,91,95
+3VSUS		+3VSUS	7,21,22,23,24,26,28,30,31,33,36,48,51,53,68,74,81,88,92,96
+3V		+3V	24,57,68,91,92
+3VS		+3VS	7,16,21,22,23,24,28,30,31,32,33,36,44,45,48,50,51,57,74,87,88,89,91,92,96
+3VS_VGA		+3VS_VGA	57,74,91,97
+3VA		+3VA	25,30,57,66,74,81,88,97
+5VO		+5VO	81,82,83,84,91,94,95,96
+5VSUS		+5VSUS	31,56,81
+5V		+5V	7,52,57,91
+5VS		+5VS	36,48,50,51,56,57,80,87,89,91
+1.05VO		+1.05VO	82,91
+1.05VSUS		+1.05VSUS	26,82
+1.05V		+1.05V	7,10,24,32,57,80,91
+1.05VS		+1.05VS	7,10,57,91
+1.2VO_DDR		+1.2VO_DDR	83,91
+1P2V		+1P2V	7,10,16,17,18,24,57,83
+0.6VO		+0.6VO	83
+VTT_DDR		+VTT_DDR	16,17,18,57,83
+1.8VO		+1.8VO	84,91
+1.8VSUS		+1.8VSUS	21,26,53,84
+1V8_MAIN		+1V8_MAIN	48,57,70,71,72,74,75,91
+1V8_AON		+1V8_AON	57,70,74,75,87,89,91
+0.95VO		+0.95VO	94
+VCCIO		+VCCIO	3,6,7,10,94
+2.5VO		+2.5VO	95
+2P5VPP		+2P5VPP	16,17,18,57,95
+PEX_VDD		+PEX_VDD	57,70,73,96
+NVVDD		+NVVDD	57,75,87
+FBVDDQ		+FBVDDQ	57,71,76,77,89
+NVVDDS		+NVVDDS	
+VCORE		+VCORE	9,80
+VCCGT		+VCCGT	9,80
+VCCSA		+VCCSA	10,80

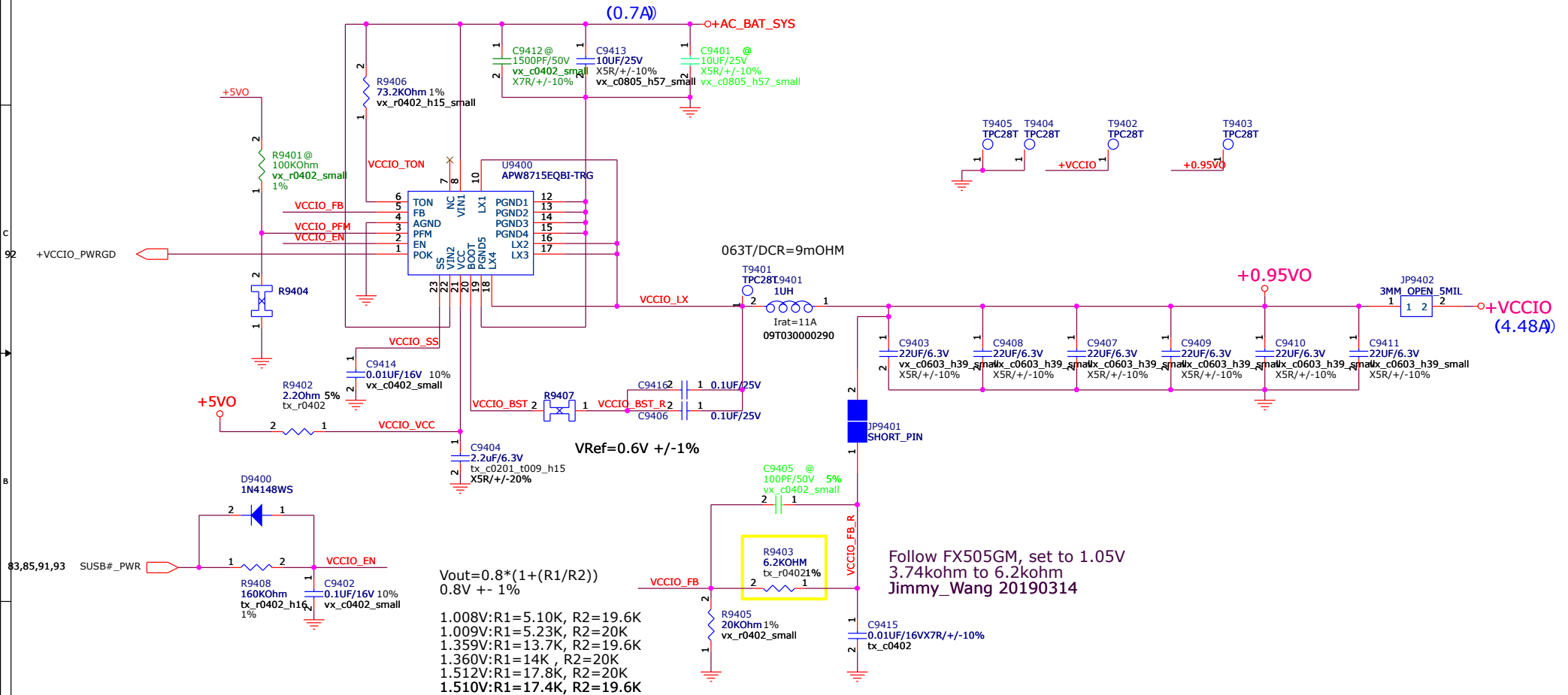
## FOR POWER TEST



<b>PEGATRON</b>		Title : <b>Signal</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL		Pegatron Corp.	
Size : <b>Custom</b>		Project Name : <b>G15G</b>	
Date : <b>Friday, March 22, 2019</b>		Rev : <b>1.0</b>	
Sheet : <b>93</b>		of : <b>108</b>	

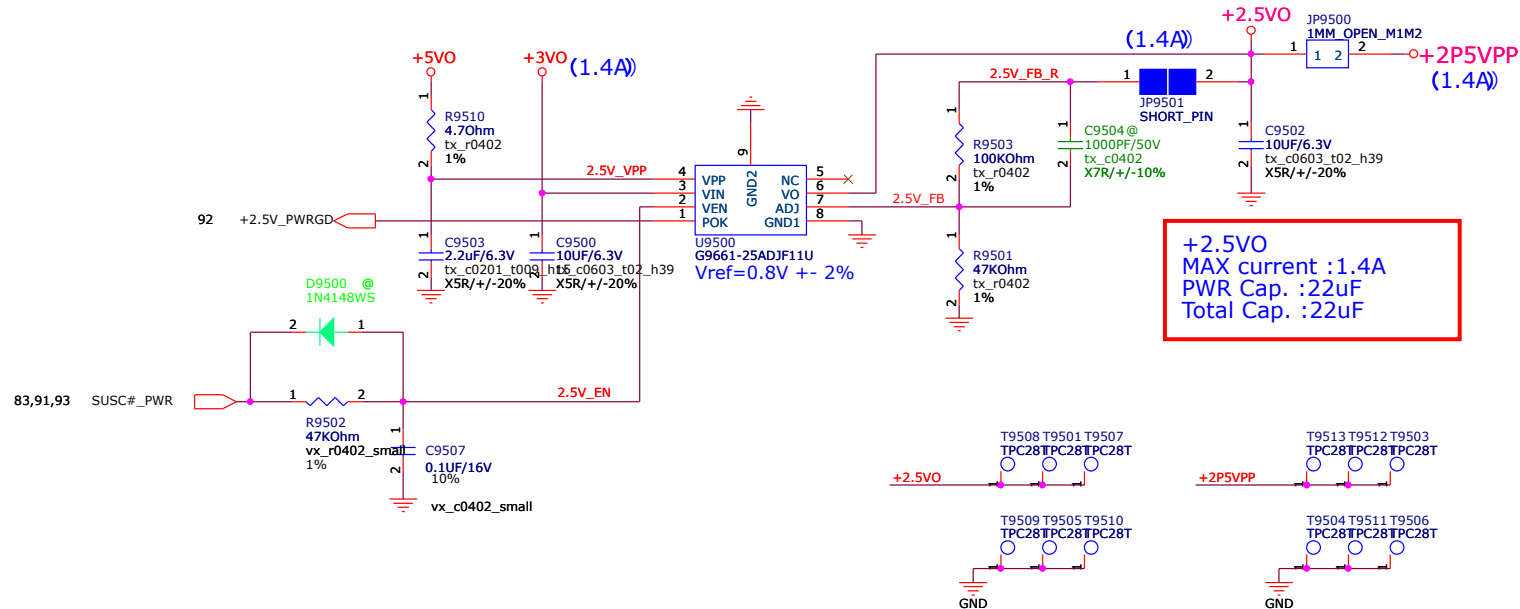


## +VCCIO POWER SUPPLY





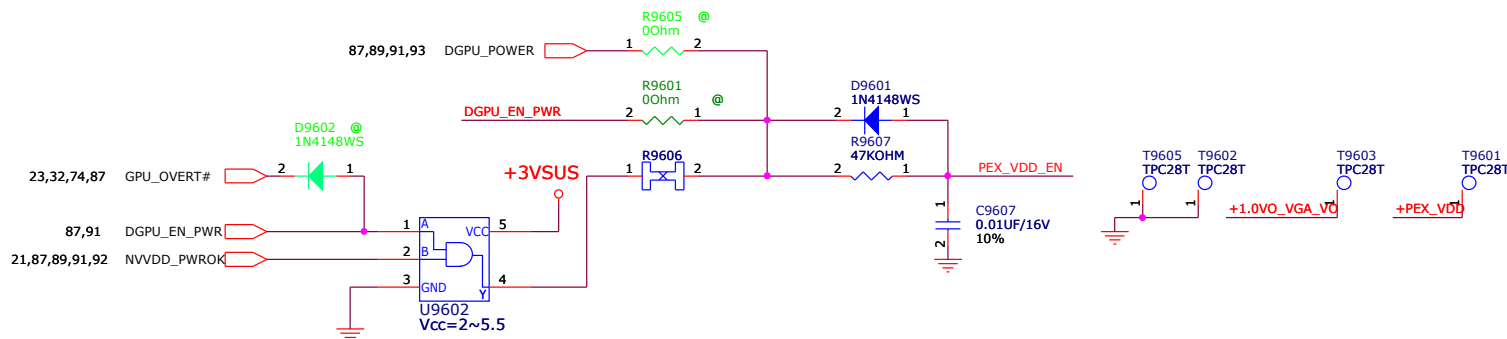
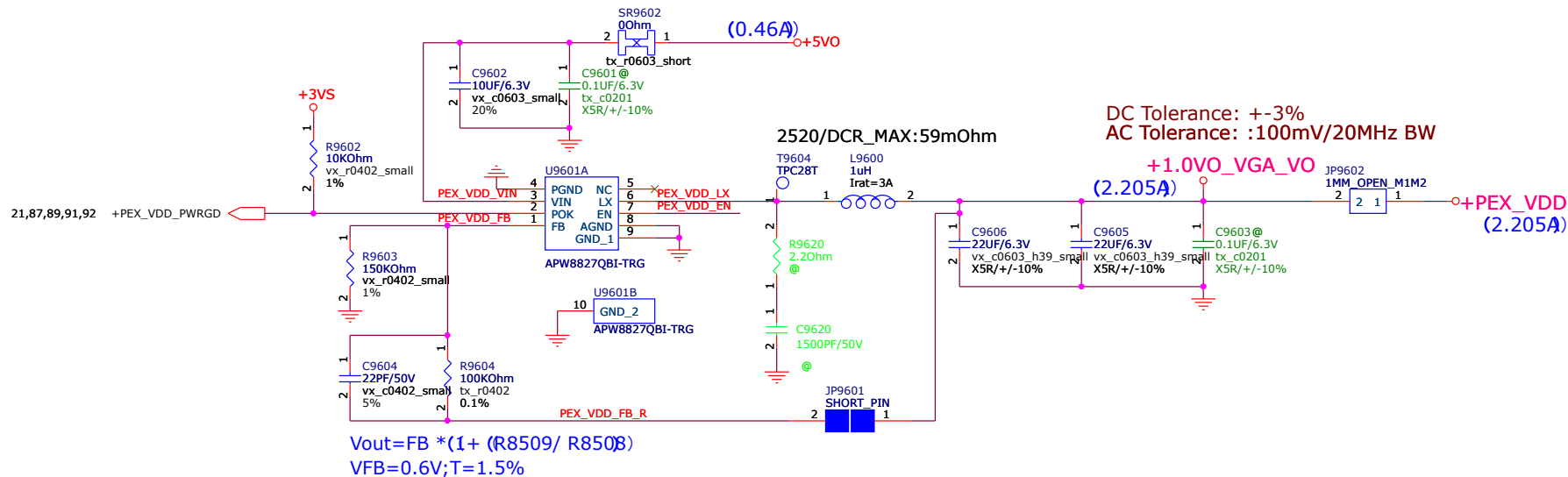
## +2.5V POWER SUPPLY



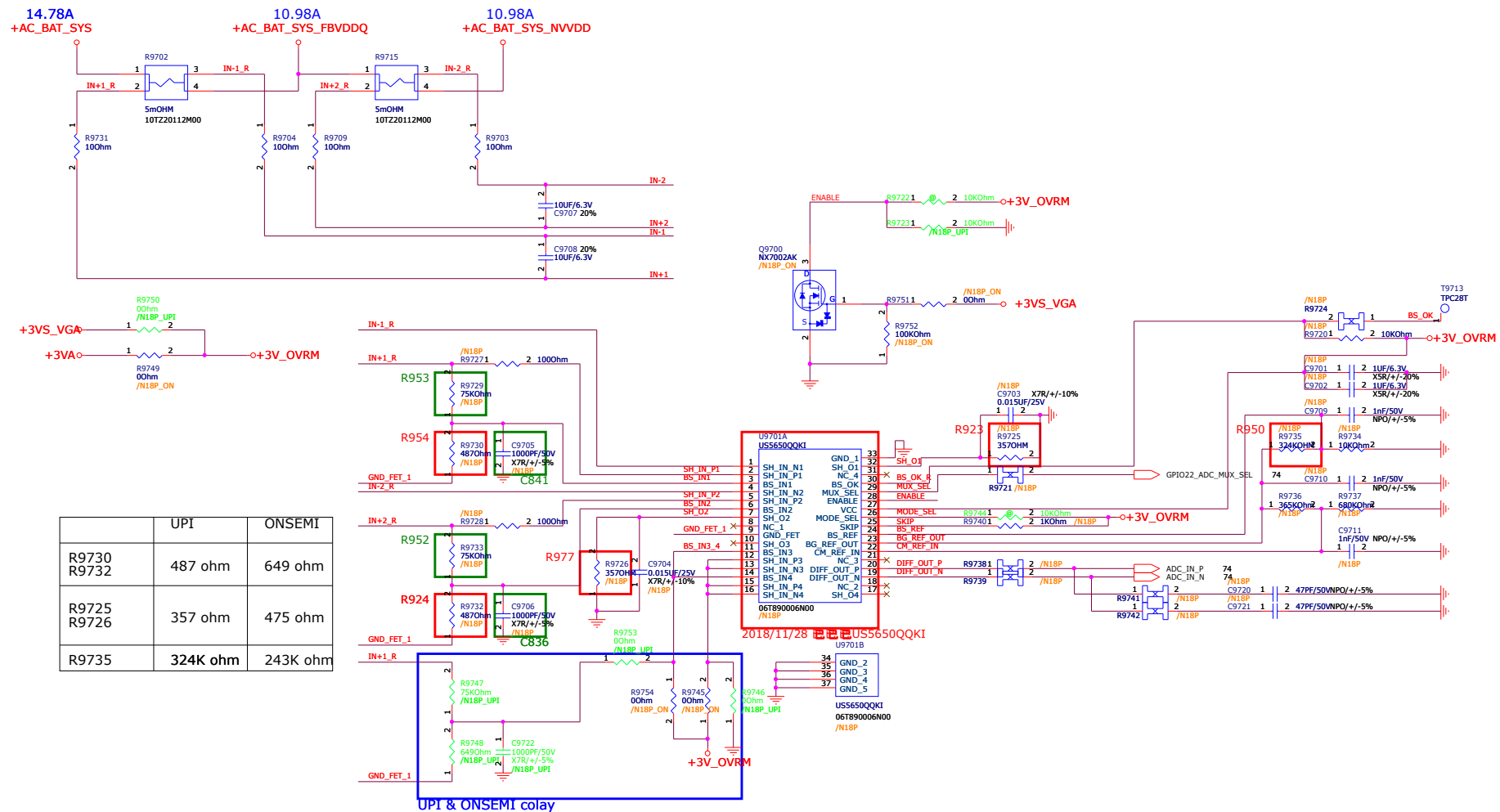


# +PEX\_VDD POWER SUPPLY

Page96 change solution  
G9661 to APW8827 for rising time issue  
Jimmy\_Wang 20190315







	UPI	ONSEMI
R9730 R9732	487 ohm	649 ohm
R9725 R9726	357 ohm	475 ohm
R9735	324K ohm	243K ohm

Table 12. Power Monitoring with OnSemi OVR-M

	Component Values				
GPU	R954, R924	R977, R923	R950	R953, R952	C841, C836
N18P-G0	649 Ω	475 Ω	243 kΩ	75 kΩ	1.0 nF
N18P-G0					
MAX-Q					

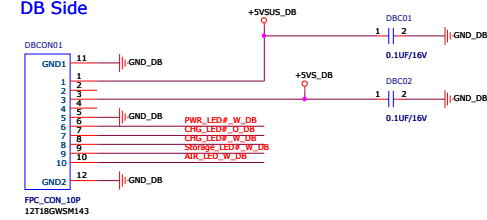
Table 13. Power Monitoring with uPI OVR-M

	Component Values				
GPU	R954, R924	R977, R923	R950	R953, R952	C841, C836
N18P-G0	487 Ω	357 Ω	324 kΩ	75 kΩ	1.0 nF
N18P-G0					
MAX-Q					

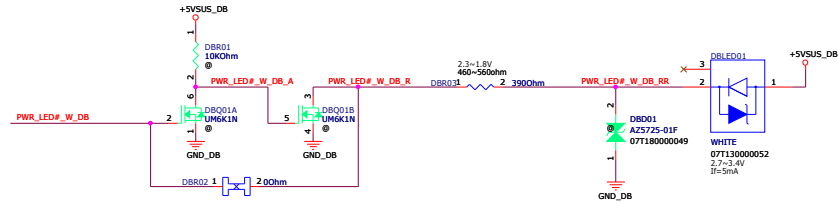






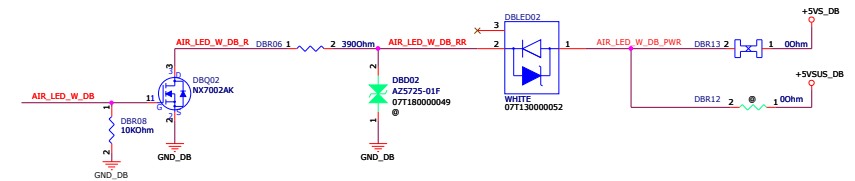


## Power LED

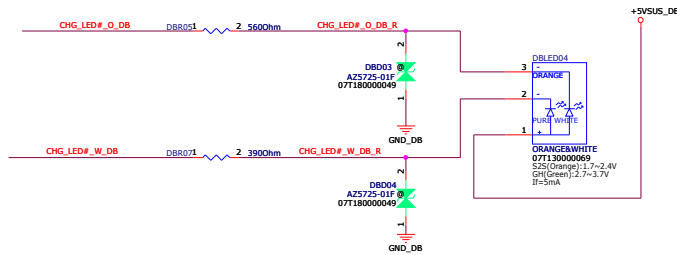


AIR PLANE LED(White)

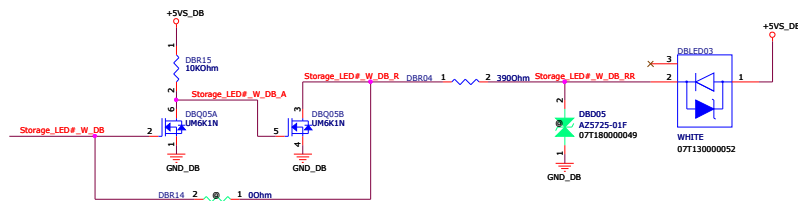
NOTE: AIR\_LED#\_R  
High -> airplane mode ON -> LED ON  
Low -> airplane mode OFF -> LED OFF



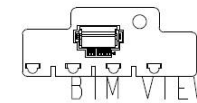
Charger LED(White/Orange)



## HDD LED



## PCB/ID LOCATION



### Tooling Hole

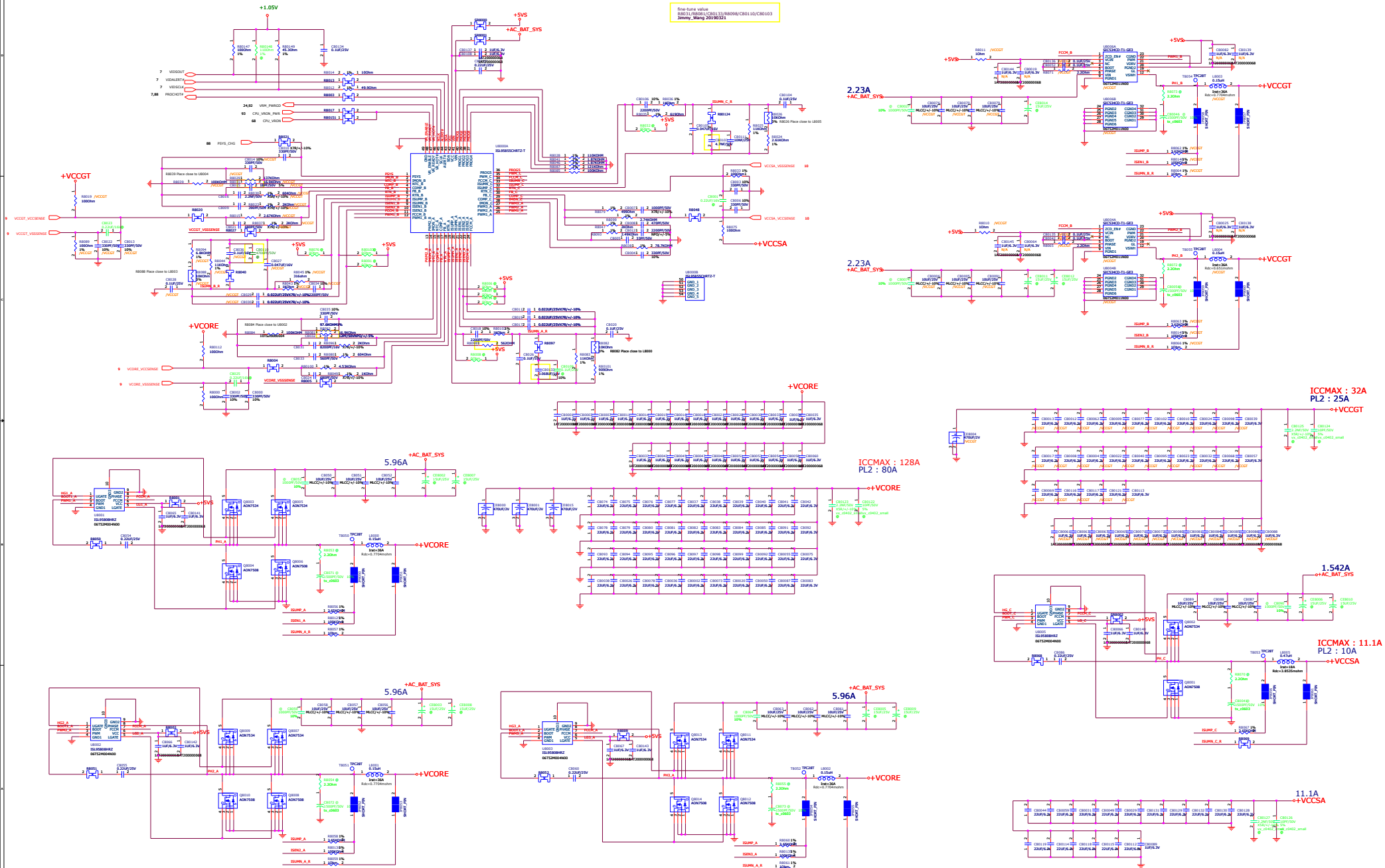
PWR\_LED  
DBLED01Charger LED  
DBLED04HDD LED  
DBLED03RF LED  
DBLED02







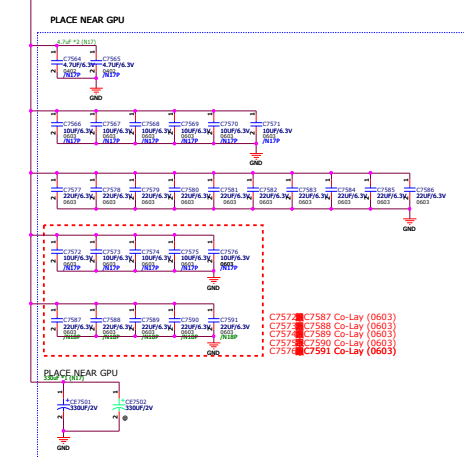
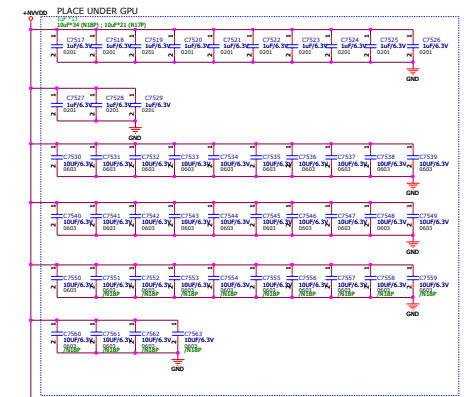
fine-tune value  
R8031/R8081/C80133/R8098/C80110/C80103  
Jimmy\_Wang 20190321











NVIDIA (N17P)  
DA-07679-001\_v05 P.40

Table 2. NVVDD Decoupling and Filtering

GPU	Capacitor Type	Footprint	Population			
			N18	N17	Location	
NVYDD Supply Net						
GB4C-128, GB4D-128	10 $\mu$ F	X65	0603	34	21	Under GPU
	1 $\mu$ F	X65	0402 or 0201W	23	43	Under GPU
	10 $\mu$ F	X65	0603	0	11	Heat GPU
	22 $\mu$ F	X65	0603	15	10	Heat GPU
	4.7 $\mu$ F	X65	0603	0	2	Heat GPU
	330 $\mu$ F	POS	7433	0	1	Heat GPU

Note:

1. Design may alternatively use two 0201W 0.47  $\mu$ F X65 for each 0201W 1  $\mu$ F.